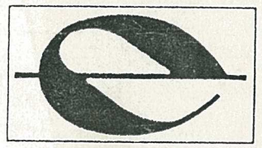
ELECTRONIC ACCORDION

DIGISYZER

Serial № 310908
made by → KAW ~~FF~~ AI



EXCELSIOR

service manual

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2. SEMICONDUCTORS LIST

IC

Code No.	Name	Description
06025	CD4001BP	Quad 2-Input positive NOR Gate
06028	CD4051B	Single 8-channel Multiplexer/Demultiplexer
06029	CD4069	Hex Inverter
06031	CD4071B	Quad 2-Input OR Gate
06032	CD4081B	Quad 2-Input AND Gate
06042	CD4013B	Dual D-Type Flip-Flop
06043	CD4019B	Quad AND-OR Select Gate
06051	CD4050B	Non Inverting Type Hex Buffer/Converters
06062	CD4028B	BCD-to-Decimal Decoder
06069	TL 082CP	J-FET Input OP-Amp
06071	MN3009	256 Steps BBD
06077	NJM4558DD	Dual OP-Amp
06080	CD4049B	Hex Inverter
06086	MC-14066BB	Quad Bilateral Switches
06903	CD4024B	7-stages Binary Counter
06906	CD4053B	Triple 2-Channel Multiplexer/Demultiplexer
06930	C-1555	Timer
06933	upd8243C	I/O Expander
06934	T6118A	LSI for Rhythm Tone Generator
06935	T6118B	
06937	BA6110	Voltage Controlled AMP
06957	SN74LS04	Hex Inverter
06958	MB74LS00	Quad 2-Input Positive NAND Gate
06959	MB74LS02	Quad 2-Input Positive NOR Gate
06960	MB74LS08	Quad 2-Input Positive AND Gate
06961	MB74LS32	Quad 2-Input Positive OR Gate
06962	MB74LS74	Dual D-Type Positive-Edge Triggered Flip Flop
06963	MB74LS75	4-Bit Bistable Latch
06964	MB74Ls86	Quad 2-Input Exclusive-OR Gate
06965	MB74LS138	3-line to 8-Line Decoder/Demultiplexer
06966	MB74LS139	Qual 2-Line to 4-Line Decoder/Demultiplexer
06967	MB74LS157	Quad 2-Line to 1-Line Data Selector/ Multiplexer (Non-Inverted Outputs)
06968	MB74LS174	Hex D-Type Flip Flop With Common Direct Clear
06969	MB74LS283	4-Bit Binary Full Adder with Fast Carry
06970	MB74LS367	Hex Bus Driver (Non Inverted 3-State Outputs. 4-Line,2-line Enable Inputs)
06971	MB74LS368	Hex Bus Driver (Inverted 3-State Outputs. 4-Line,2-Line Enable Inputs)
06972	MB62106C	LSI for T-C-2 Circuit
06973	MB62107C	LSI for NR Circuit
06974	MB63104M	LSI for HCC Circuit
06975	MB63105C	LSI for TC-1 Circuit
06976	MB60119C	LSI for WFG Circuit
06977	MB60120C	LSI for FNG Circuit
06978	MB60121C	LSI for ADSR Circuit
06979	MB60122C	LSI for WFG circuit
06980	MB2114A-10LM	N Channel Silicon Gate MOS Memory: 4096Bits Static Random Access
06982	MB84011B	Quad 2-Input Nand Gate
06983	MB84013B	Dual D-Type Master Slave Flip Flop
06984	MB84051B	Single 8-Channel Multiplexer/Demultiplexer
06985	MB840538	Triple 2-Channel Multiplexer/Demultiplexer
06986	upd8253C5	Programmable Interval Timer
06987	upd8039LC	1 chip 8 Bit Microcomputer
06988	upd780C-1	8Bit Microprocessors
06989	TC40H174P	Hex D-Type Flip-Flop (Silicon Monolithic)
06990	TA75558P	Dual OP-Amp (Low Noise)
06981	MB2114A-15LM	N-Channel Silicon Gate MOS Memory: 4096 Bits Static RAM: (Access time:MAX 150ns)
06991	MB84024B	7-Bit Ripple-Carry Binary Counter
06992	MB84070B	Quad Exclusive-OR Gate
06993	MB74LS161	Synchronous 4-Bit Binary Counter
06994	MB74LS175	Quad D-Type Flip-Flop With Common Direct Clear, Complementary Outputs
06996	MB74LS374	Octal Positive Edge-Triggered D-Type Flip-Flop with 3 State Outputs
06997	TA7630P	2-Channel DC Control IC
06999	upc393	Dual Comparator
07004	upc7805	Voltage Regulator +5 V
06074	upc7815	Voltage Regulator +15 V
07007	upc7905	Voltage Regulator -5 V
06083	upc7915	Voltage Regulator -15 V
07006	TL321	Dual OP-AMP
06912	CD40174B	Hex D-Type Flip-Flop with Common Direct Clear
07008	SN74LS174	Hex D-Type Flip-Flop with Common Direct Clear
06016	RC4558DN	Dual OP-AMP
06054	CD4520B	Dual 4-Bit Up Counter
06920	CA3280G	Dual Voltage Controled AMP
06921	RC4136	Quad OP-AMP
83370 (1P08)	MB7054	P-ROM(1024*4)
83380 (1P09)	MB7054	P-ROM(1024*4)
83390 (1P10)	MB7054	P-ROM(1024*4)
83400 (1P11)	MB7054	P-ROM(1024*4)
83410 (1P12)	MB7054	P-ROM(10 4*4)
83420 (1P13)	MB7054	P-ROM(1024*4)
83430 (1P14)	MB7054	P-ROM(1024*4)
83440 (1P15)	MB7054	P-ROM(1024*4)
83450 (2P18)	MB8333	MASK ROM(4096*8)
83460 (1P19)	MB8364	MASK ROM(8192*8)
83471 (1P20)	TMS2564	EP-ROM(8192*8) MASK ROM MB8364(Fujitsu) Compatible
83481 (1P21)	TMS2564	EP-ROM(8192*8) MASK ROM MB8364(Fujitsu) Compatible
83520 (2P24)	TMS2564	EP-ROM(8192*8) MASK ROM MB8364(Fujitsu) Compatible
83500 (2P22)	MBM2764	EP-ROM(8192*8)

Transistor

06101	2SC536F	Si NPN:Planar Type Transistor
06102	2SA564R	Si PNP:Epitaxial Planar Type Transistor
06118	2SC2838	Si NPN:120W Type SiliconMold Transistor
06136	2SC536FNoise	Si NPN:Planar Type Transistor(Noise)
06139	2SD438E	Si NPN(Power Transistor) Epitaxial Planar Type Transistor
06147	2SB560E	Si NPN:Epitaxial Planar Type Transistor
06148	2SB507	Si NPN:Triple Diffused Planar Type Transistor
06151	2SA733P	Si PNP:Epitaxial Type Transistor
06152	2SC445P	Si NPN:Epitaxial Type Transistor

Diode

06301	IS2473	Si Diode
06304	MI152	Si Rectifier
06548	DBA-60C-Z15	Si Rectifier
06549	DBA-100B	Si Rectifier
06320	RM-1Z	Si Diode

FET

06511	2SK44D	Sin Type:N-Channel Junction Type FET
06537	2SK304E	Sin Type:N-Channel Junction Type FET

Zener Diode

06311	05z47Y	4.7V
06501	WZ-061	6V

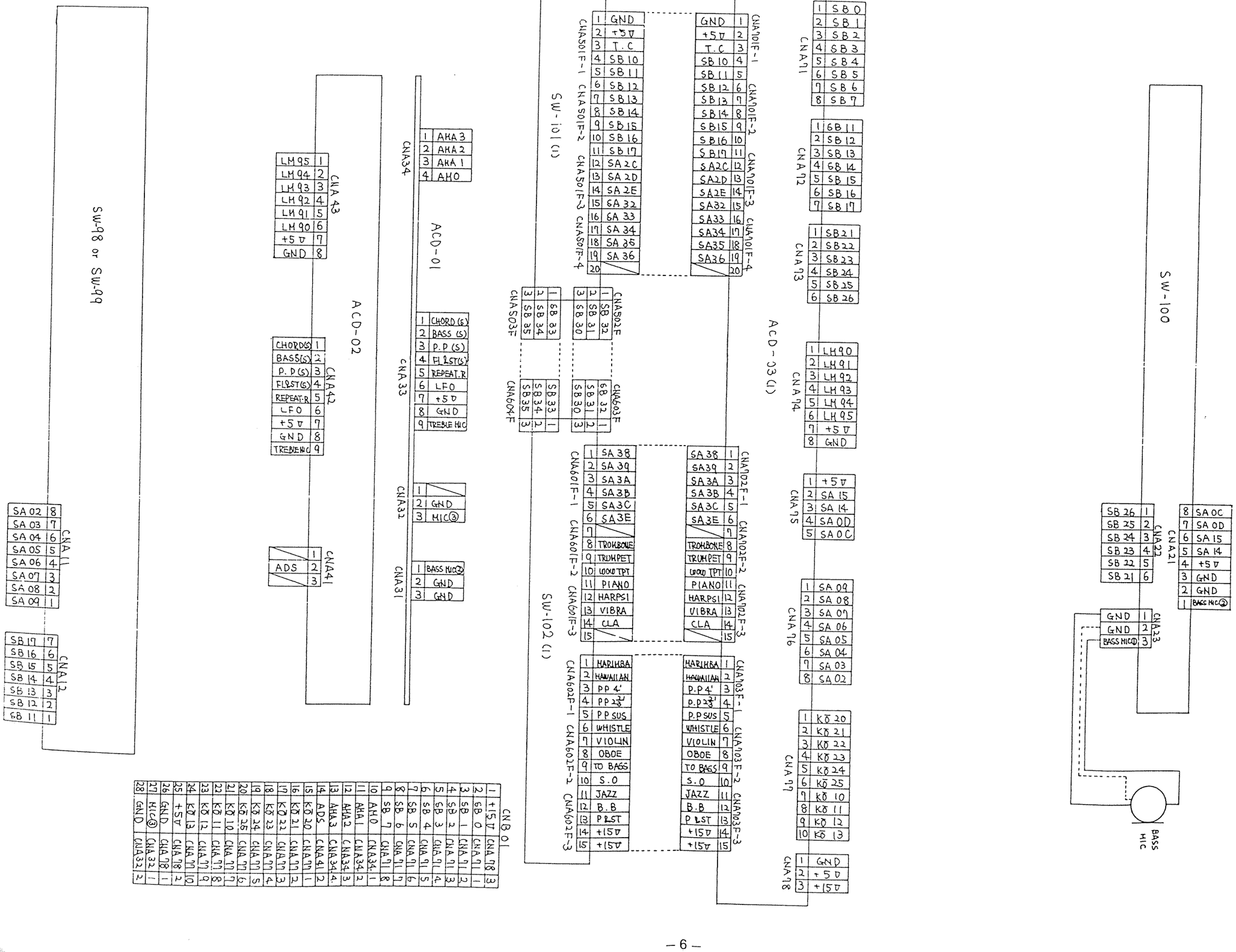
Power Transformer

11270	TSE-213D	for Japan
11271	-213U	for Canada, U. S. A.
11272	-213E	for 110V/220V Markets
11273	-213L	for Europe Markets

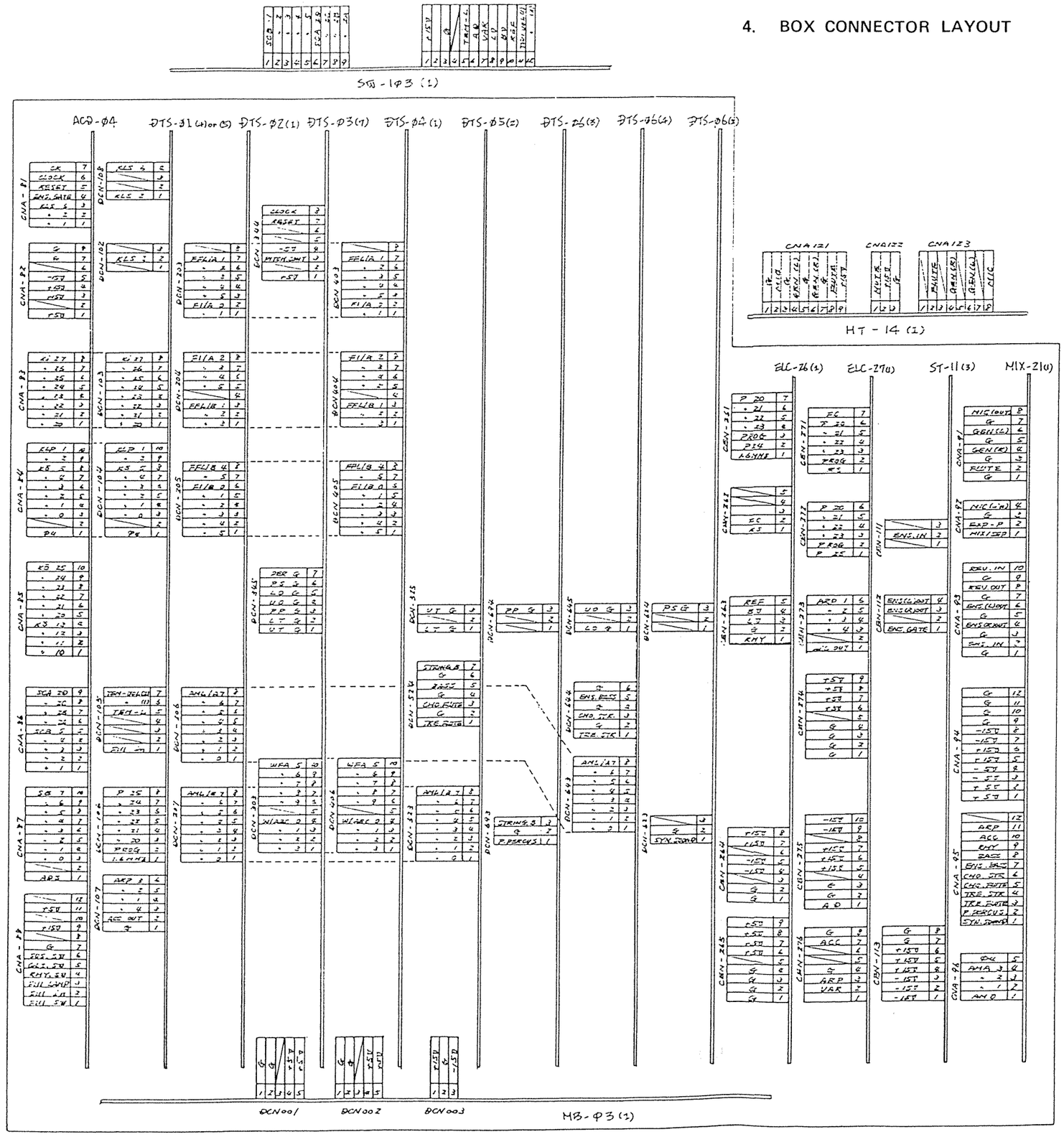
Others

06513	MCD521A	Photo Coupler
06534	SR503C	LED
06550	TF-620N	SCR

3. ACCORDION CONNECTOR LAYOUT

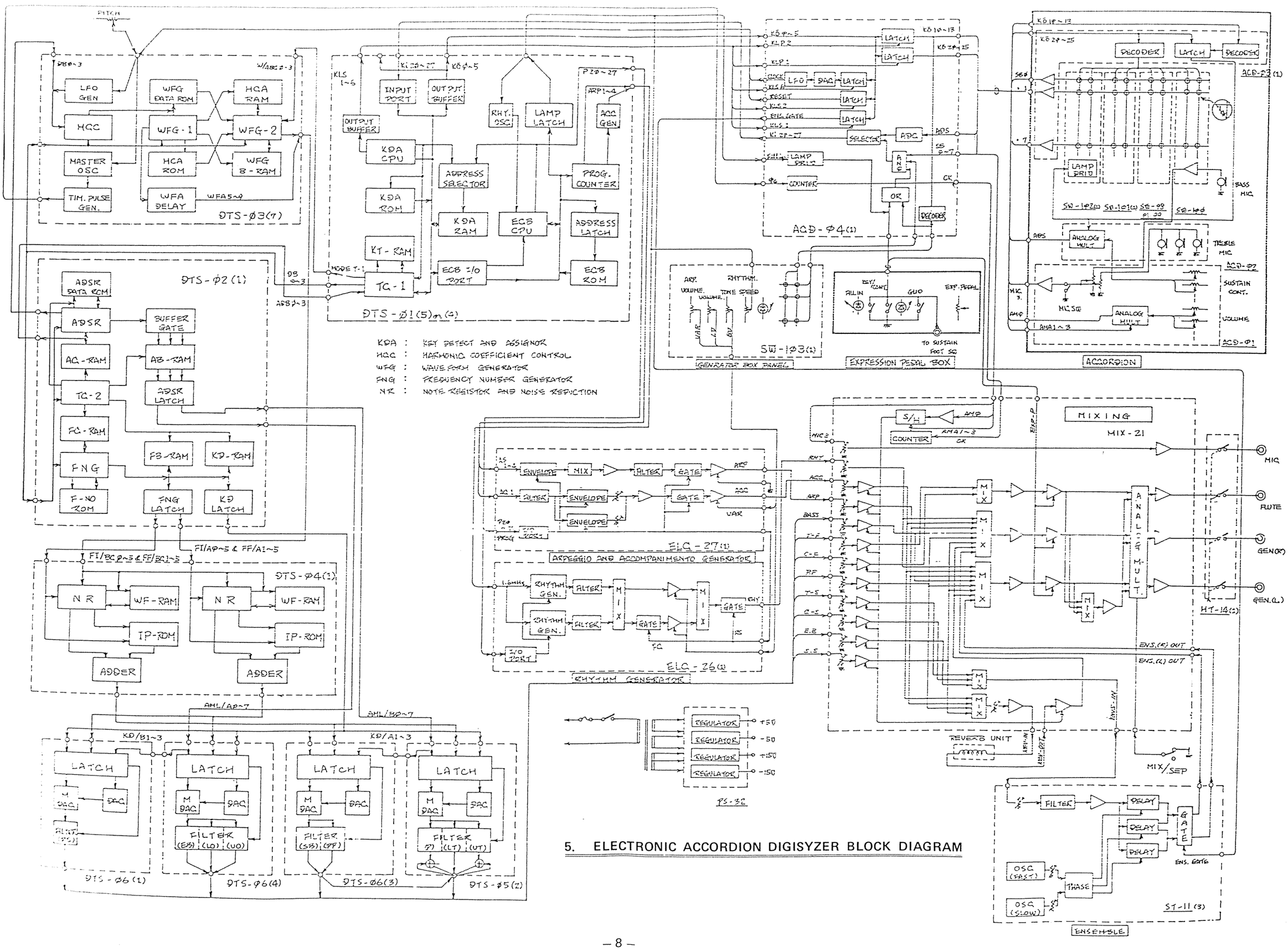


4. BOX CONNECTOR LAYOUT



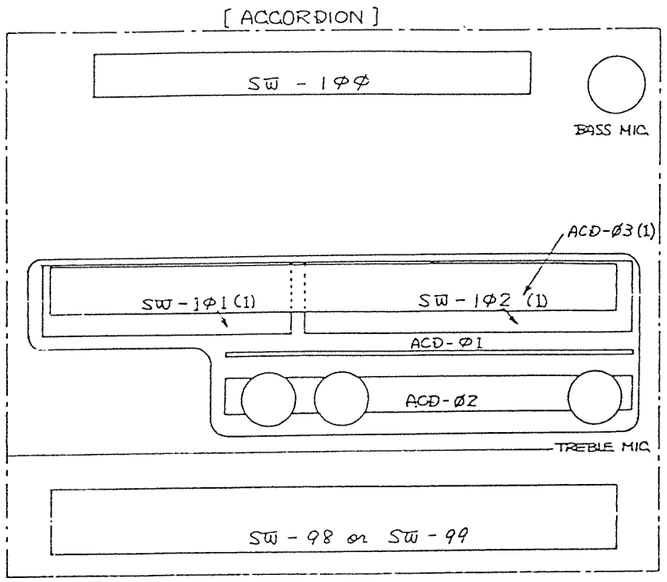
* In This Manual, The Following Terms Are The Same.

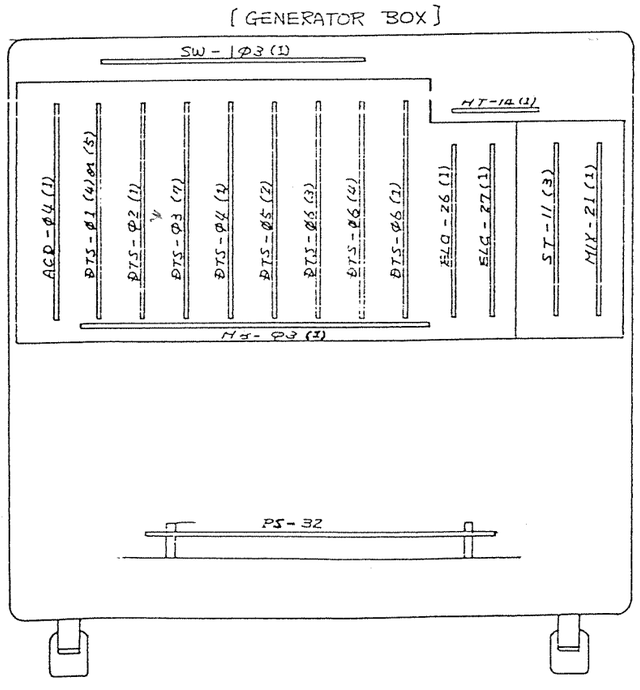
Accordion	Organ
Treble	Upper
Chord	Lower
Bass	Pedal
ECB II	ACB
Flute	Tibia
Synthe Sound	Player Sound
Strings	Orchestra

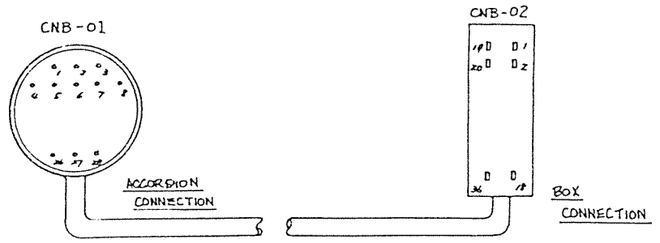


5. ELECTRONIC ACCORDION DIGISYZER BLOCK DIAGRAM

6. PRINT BOARDS LAYOUT

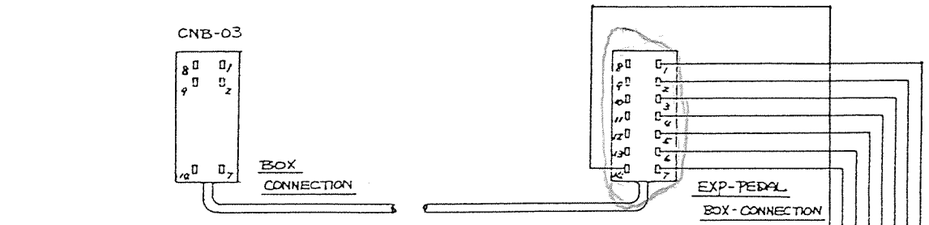




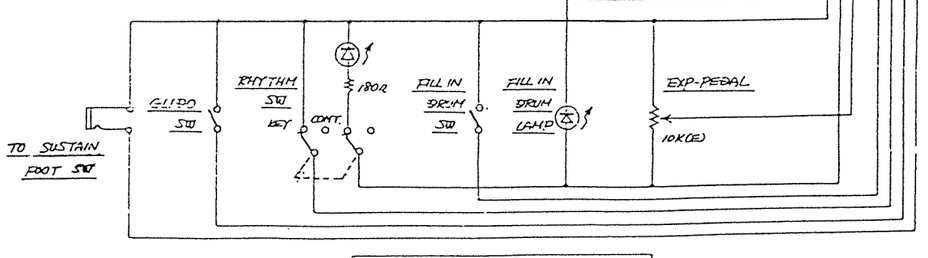


PLUG and SOCKET CHART					
n° PIN	FUNCTION	COLOR	n° PIN	FUNCTION	COLOR
1	+15V	RED	16	KB 21	Spiral RED
2	SB 0	BLACK	17	" 22	" ORANGE
3	" 1	BROWN	18	" 23	" YELLOW
4	" 2	RED	19	" 24	" GREEN
5	" 3	ORANGE	20	" 25	" BLUE
6	" 4	YELLOW	21	KB 16	" PURPLE
7	" 5	GREEN	22	" 11	" GRAY
8	" 6	BLUE	23	" 12	" WHITE
9	" 7	PURPLE	24	" 13	" PINK
10	AM 0	GRAY	25	+5V	BLUE
11	AMA 1	WHITE	26	G	WHITE
12	" 2	PINK	27	MIC	BLUE
13	" 3	LIGHT GREEN	28	Shield	
14	ADS	Spinal BLACK			
15	KB 20	" BROWN			

LOOKING AT PINS FROM FRONT



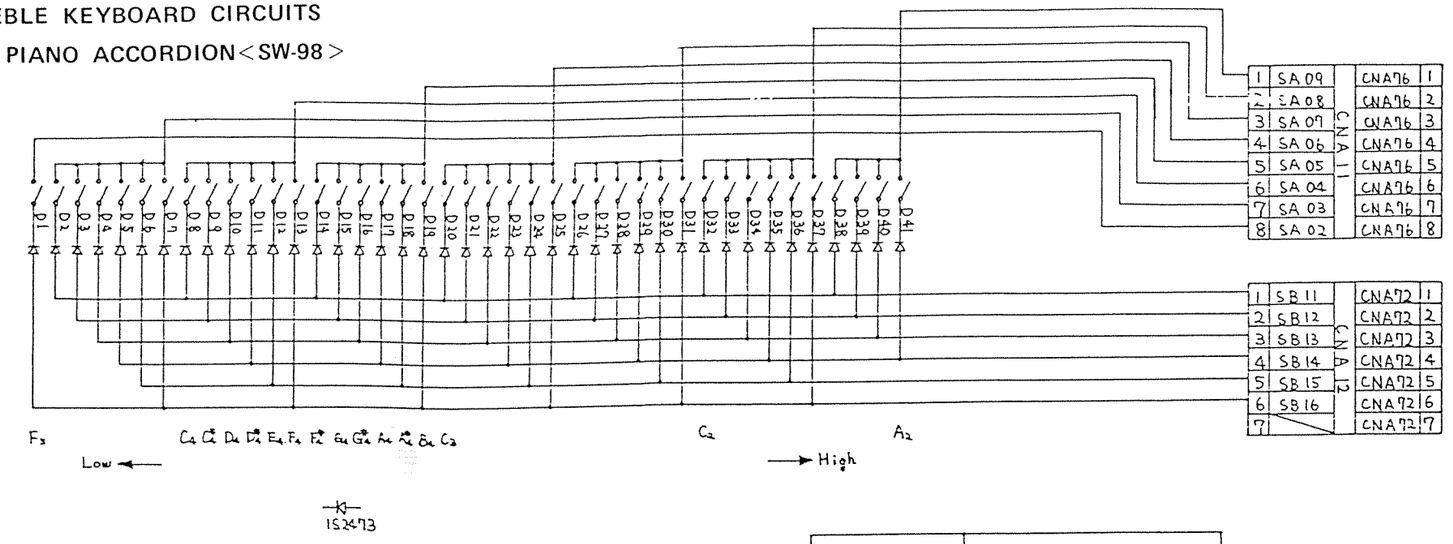
PLUG and SOCKET CHART					
n° PIN	FUNCTION	COLOR	n° PIN	FUNCTION	COLOR
1	SUS. SW	BLACK	6	EXP-PEDAL	GREEN
2	GLIDE SW	BROWN	7	+5V	BLUE
3	RHY. SW	RED	8	G	PUPLE
4	FILL SW	ORANGE	9	9	GRAY
5	FILL RAMP	YELLOW			



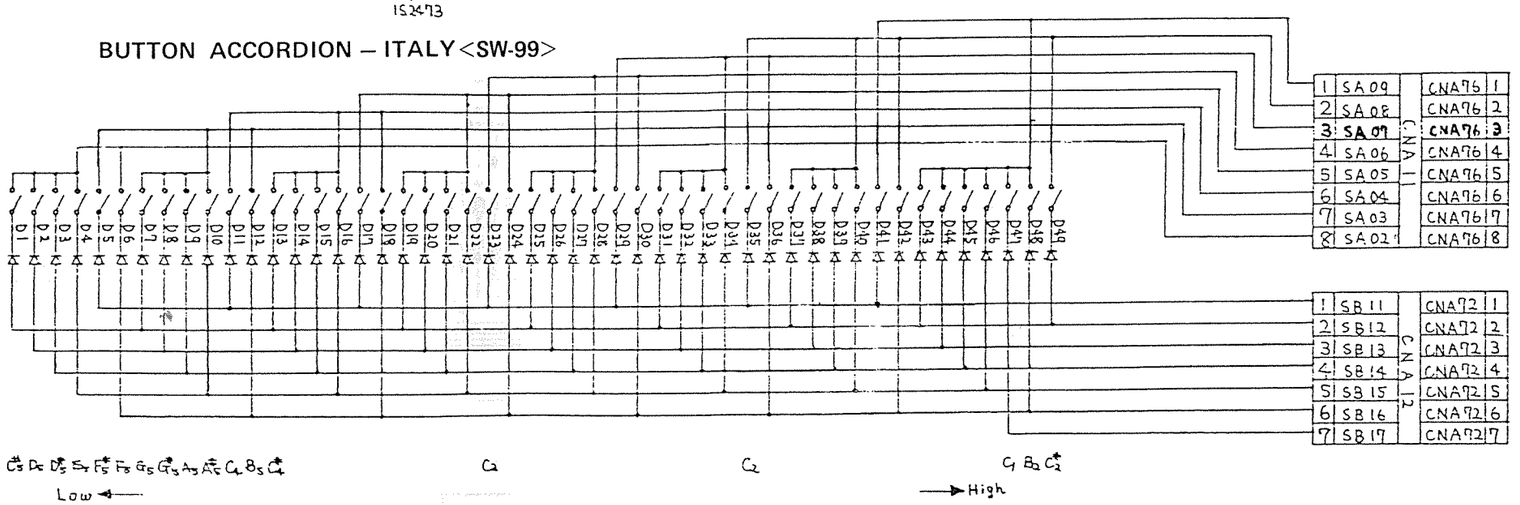
EXPRESSION PEDAL BOX

7. TREBLE KEYBOARD CIRCUITS

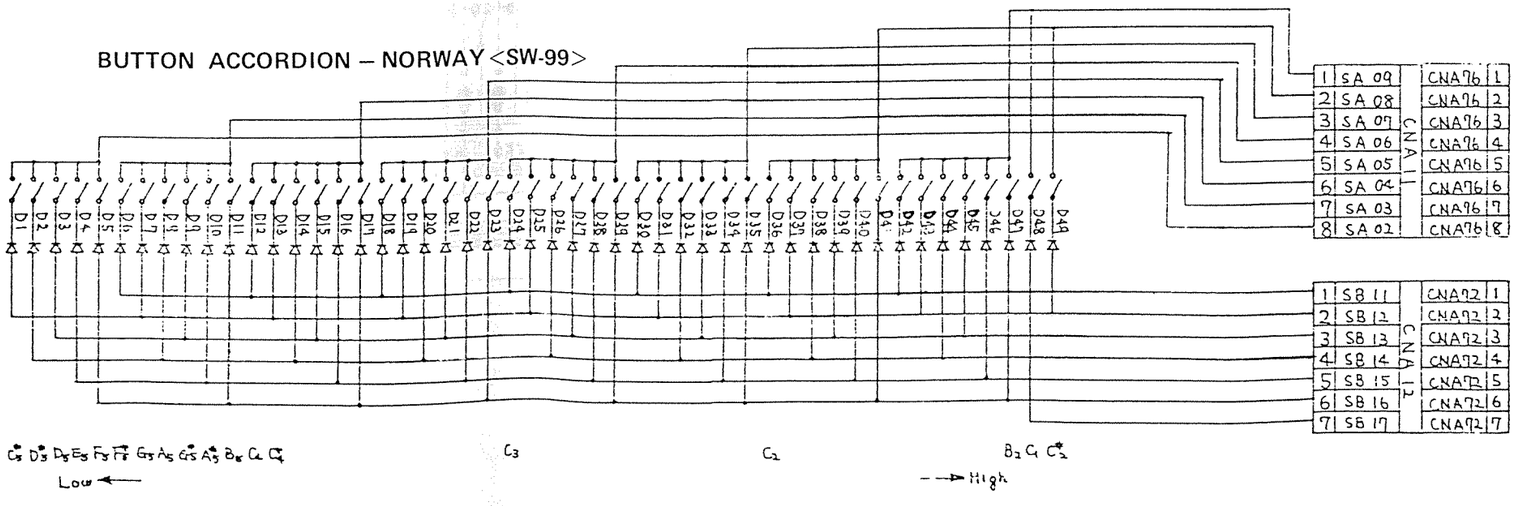
PIANO ACCORDION<SW-98>

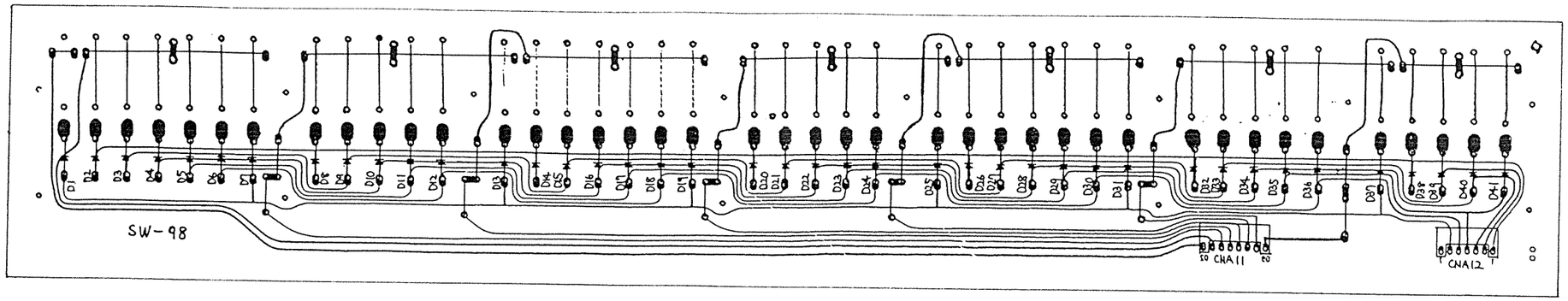


BUTTON ACCORDION – ITALY<SW-99>



BUTTON ACCORDION – NORWAY<SW-99>

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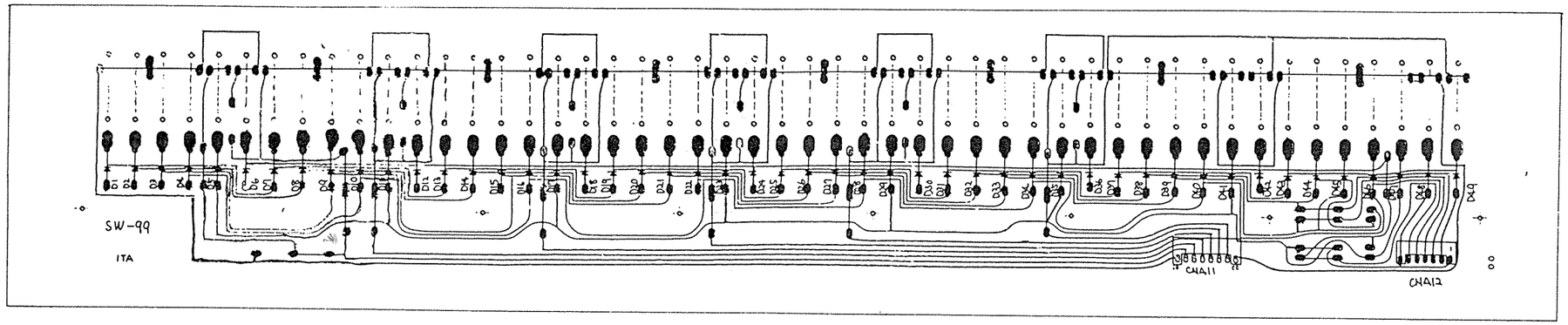
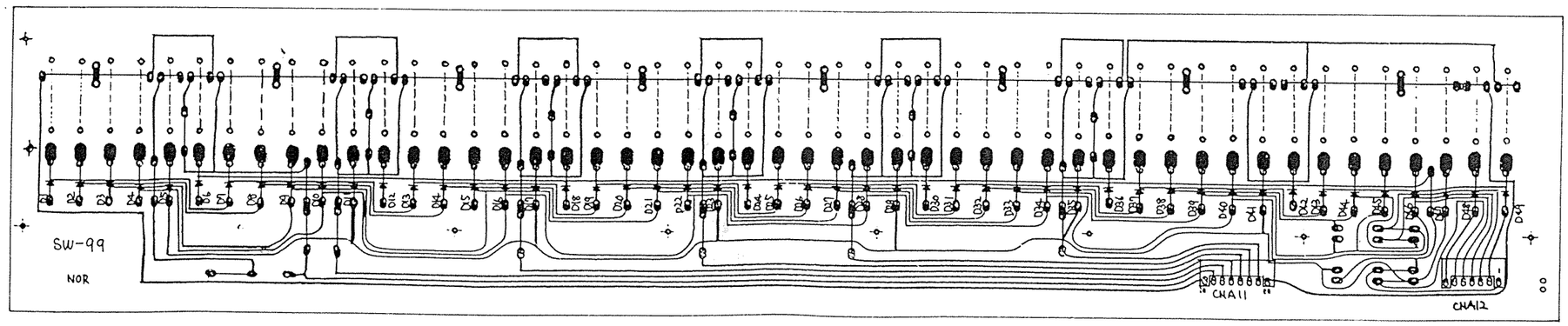
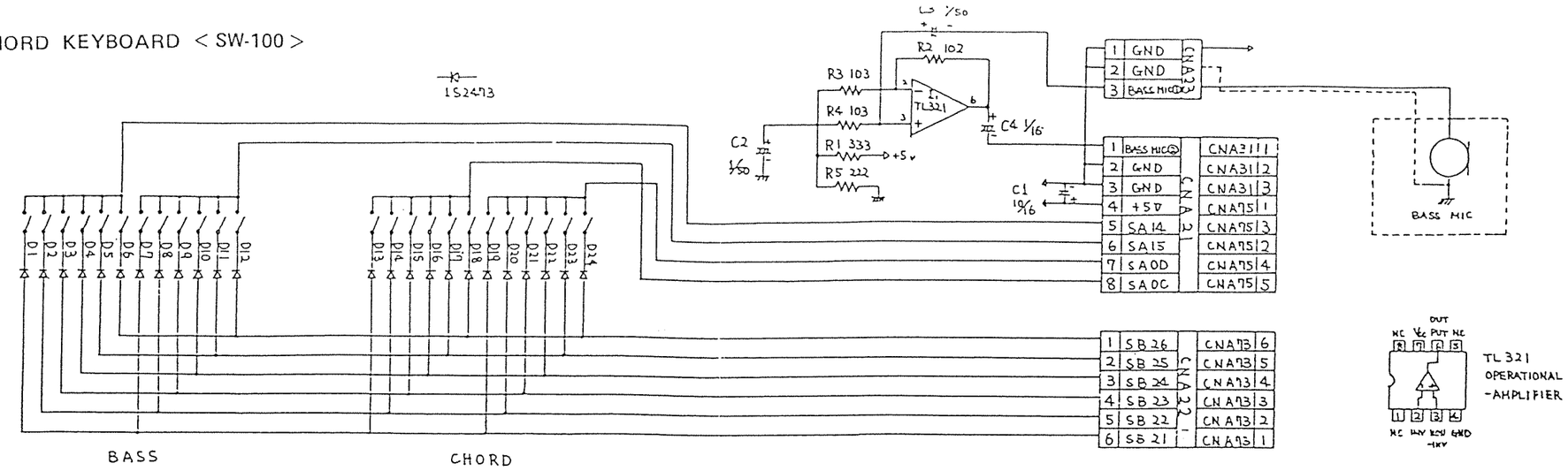
CNA12

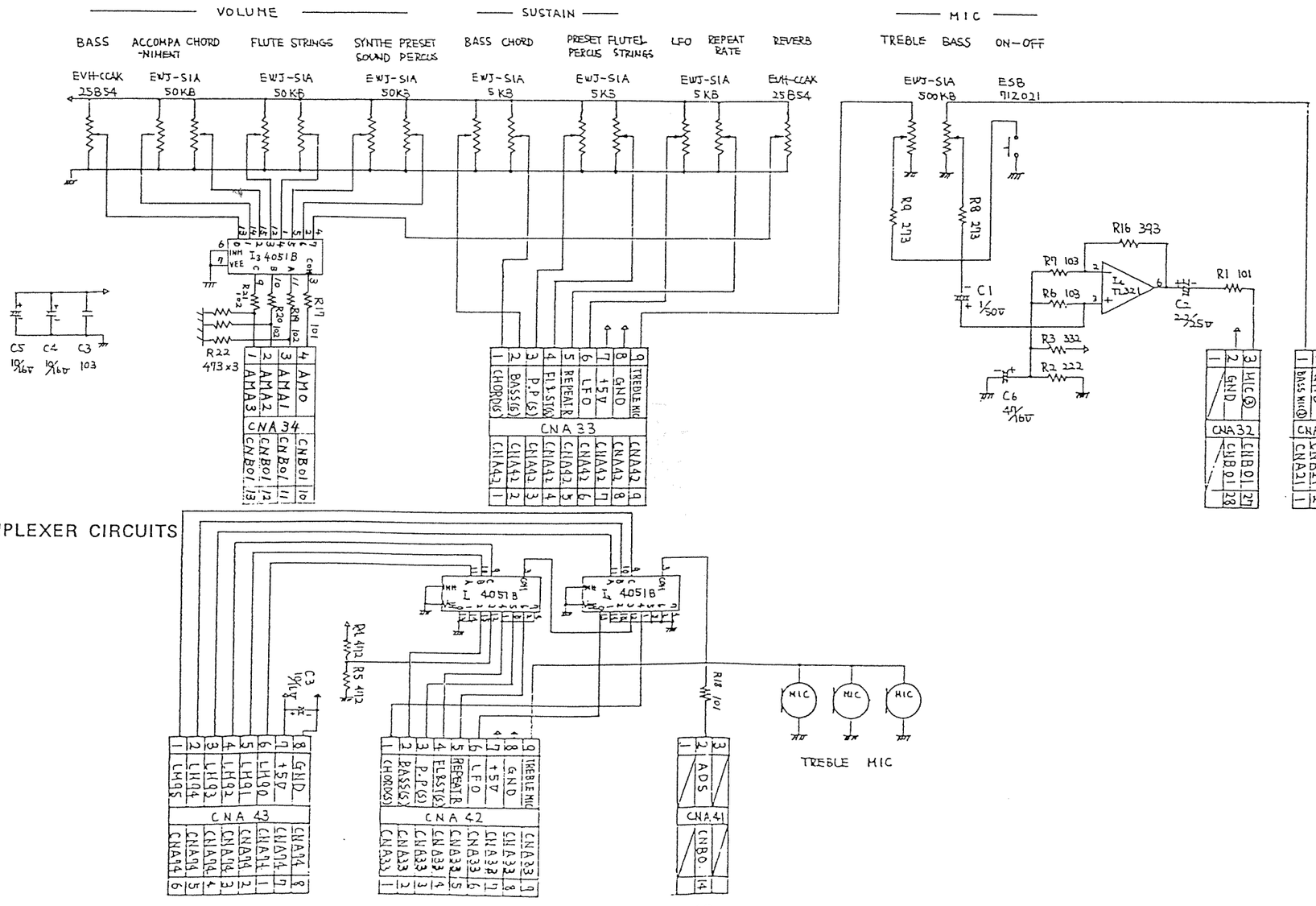

SW-99
ITA
CNA11
CNA12


SW-99
NOR
CNA11
CNA12

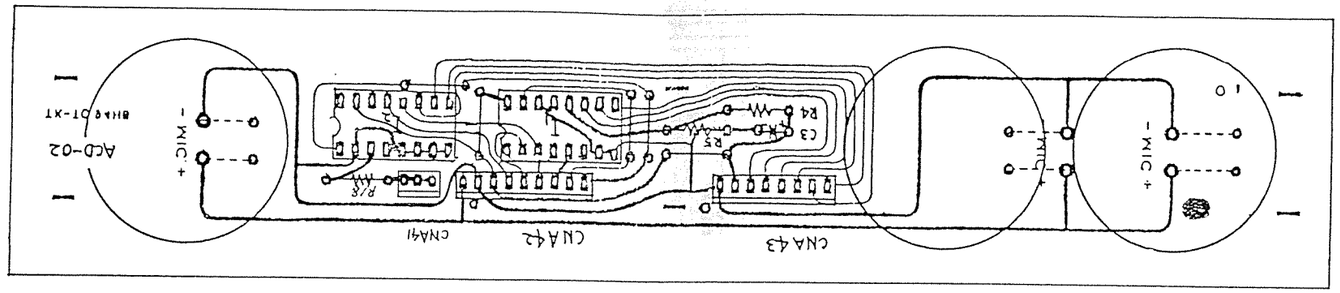
8. BASS & CHORD KEYBOARD < SW-100 >



VOLUME & SUSTAIN CONTROL < ACD-01 >



TREBLE MIC & MULTIPLEXER CIRCUITS < ACD-02 >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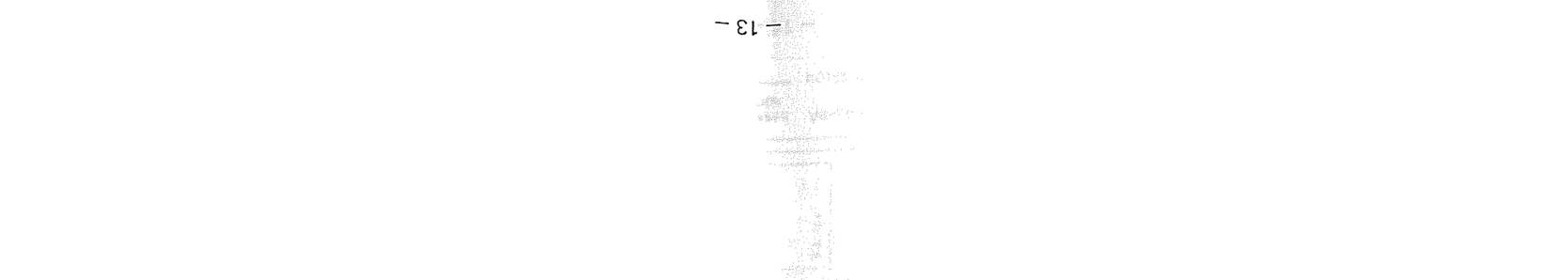
CNA42
CNA43
MIC -
MIC +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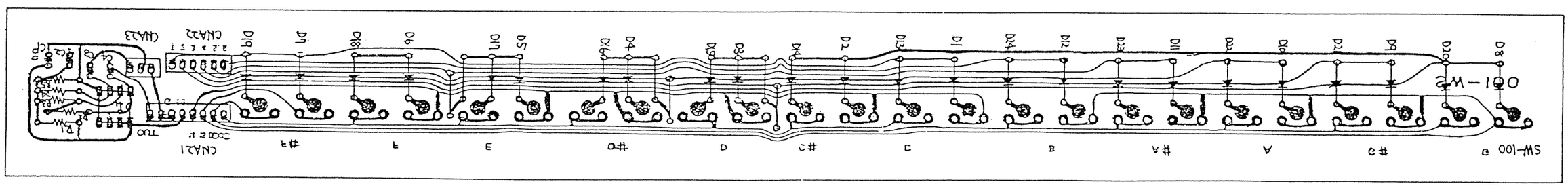
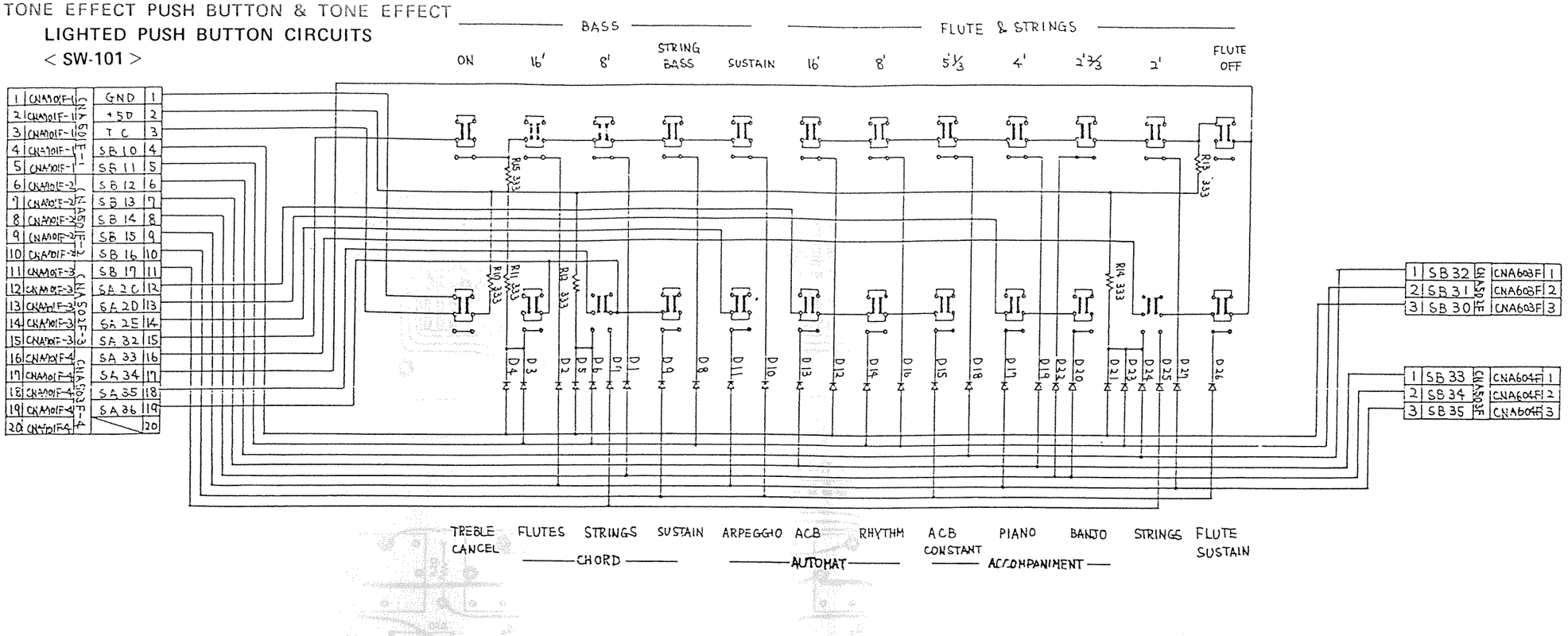
CNA 33
CNA31


SW-100
CNA21
CNA22
CNA23

9. TONE EFFECT PUSH BUTTON & TONE EFFECT LIGHTED PUSH BUTTON CIRCUITS

< SW-101 >



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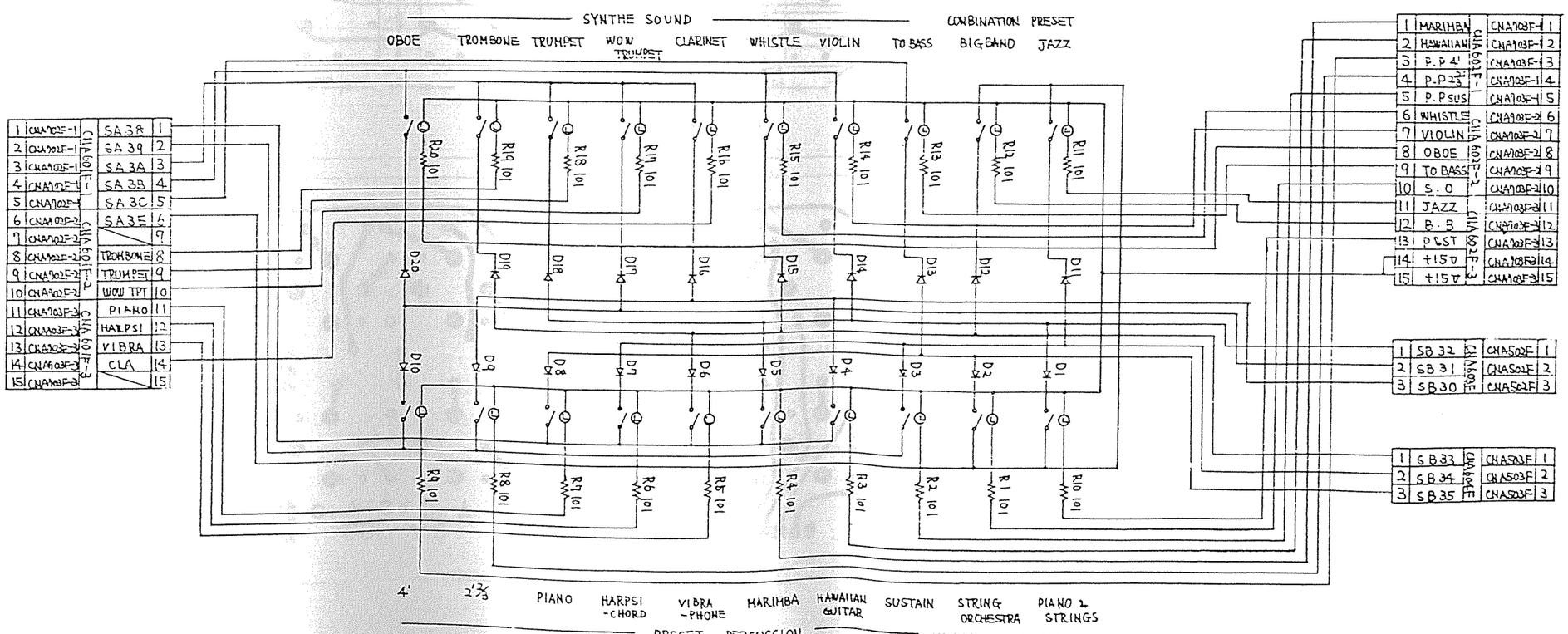

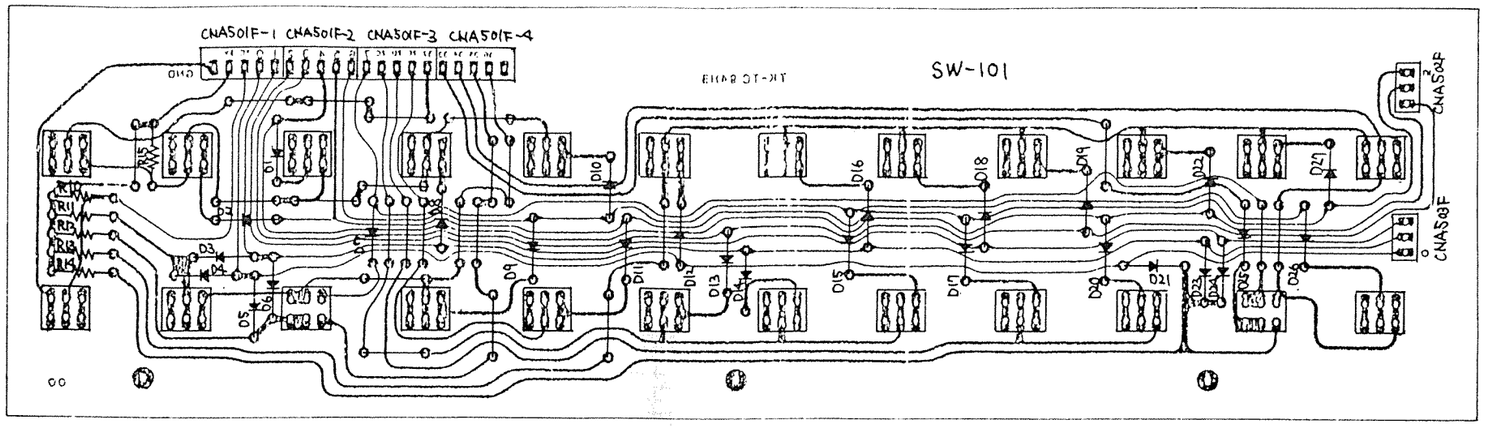
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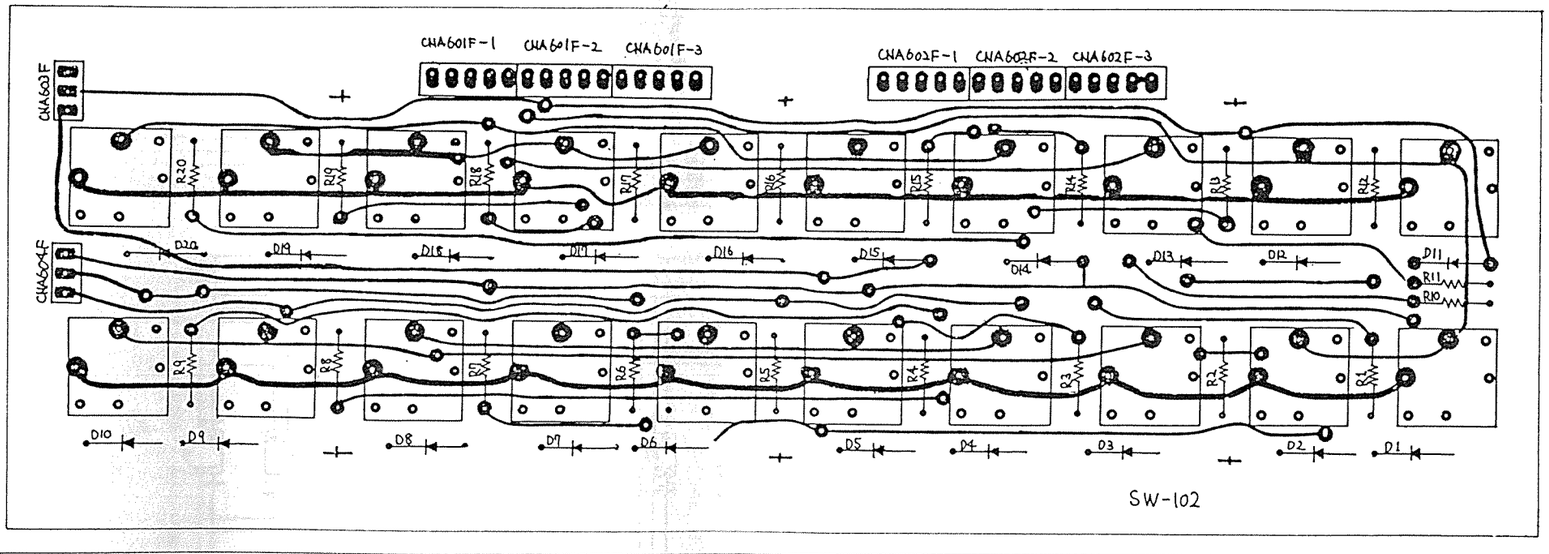
SW-101
CNA504F
CNA503F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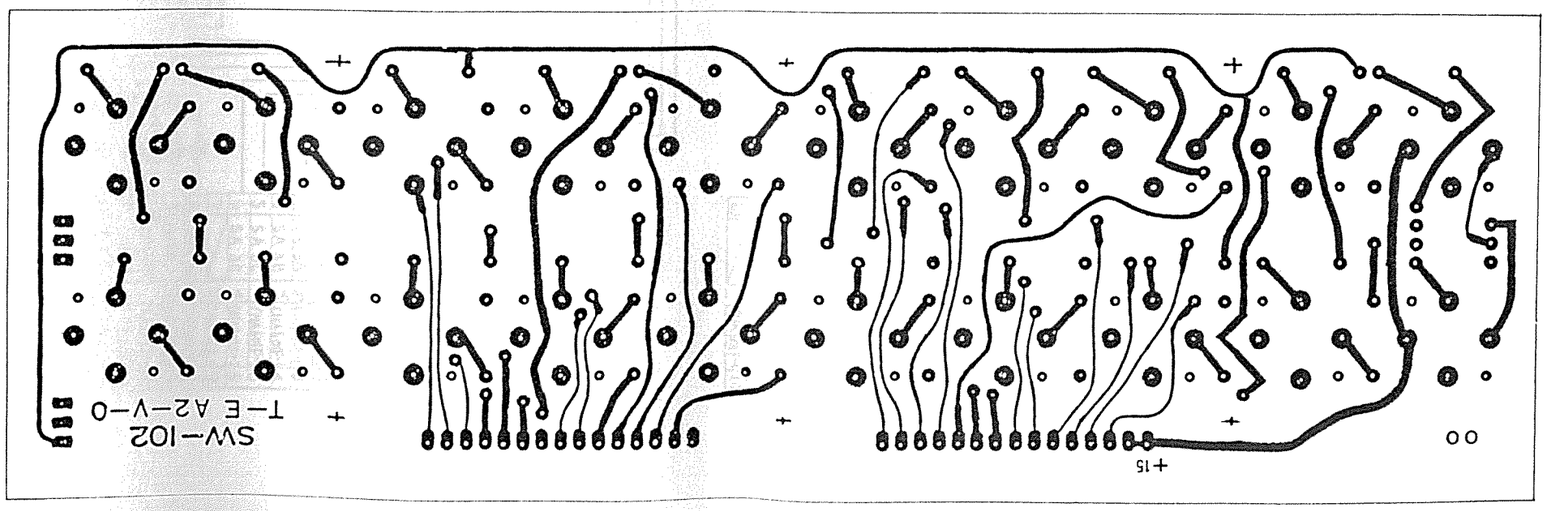
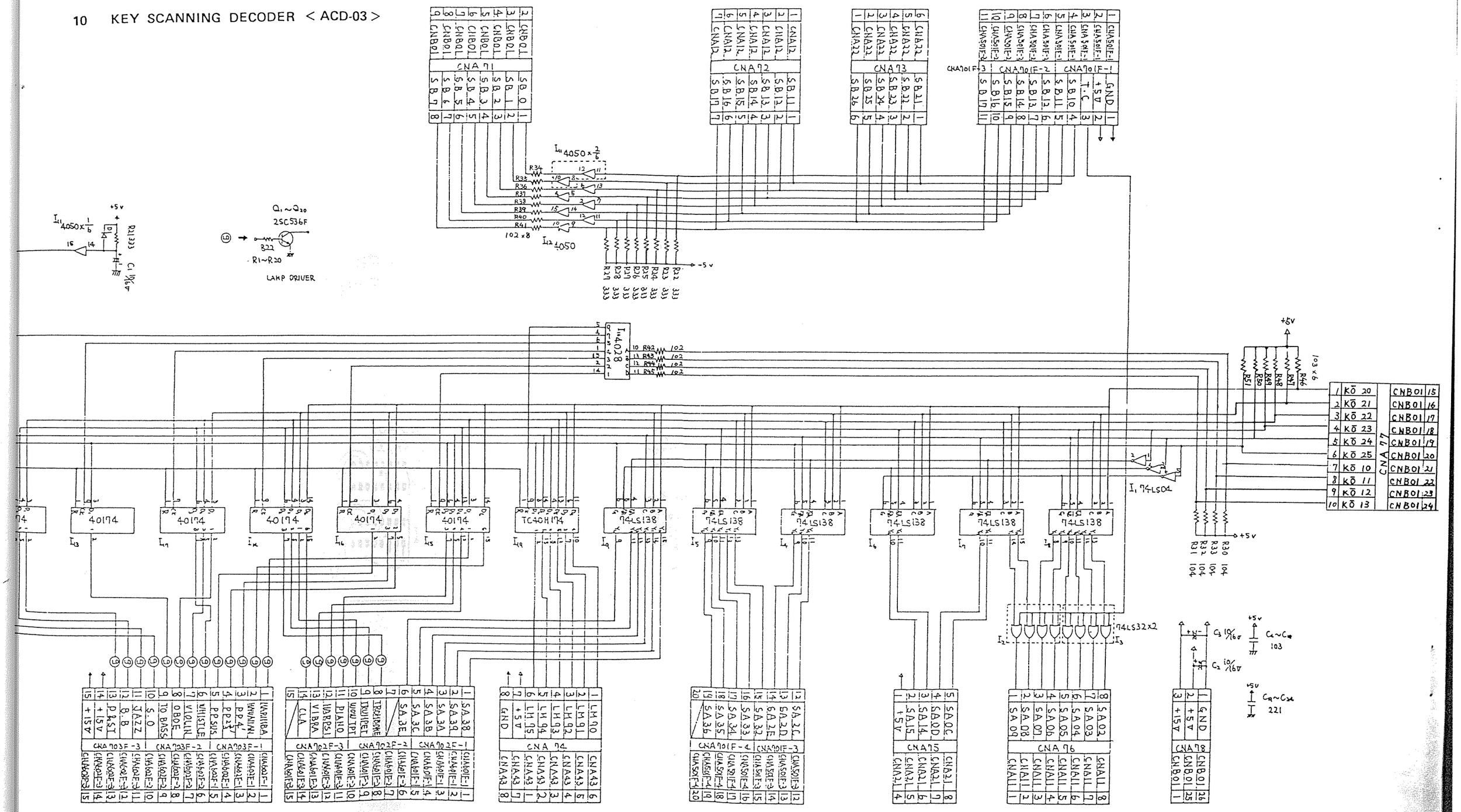
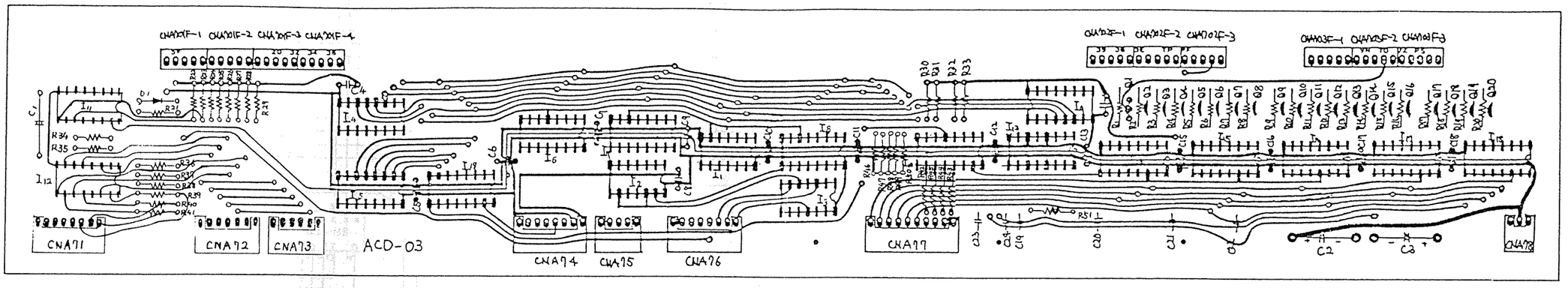
CNA603F
CNA604F
SW-102


SW-102
T-E A2-V-O

10 KEY SCANNING DECODER < ACD-03 >




ACD-03
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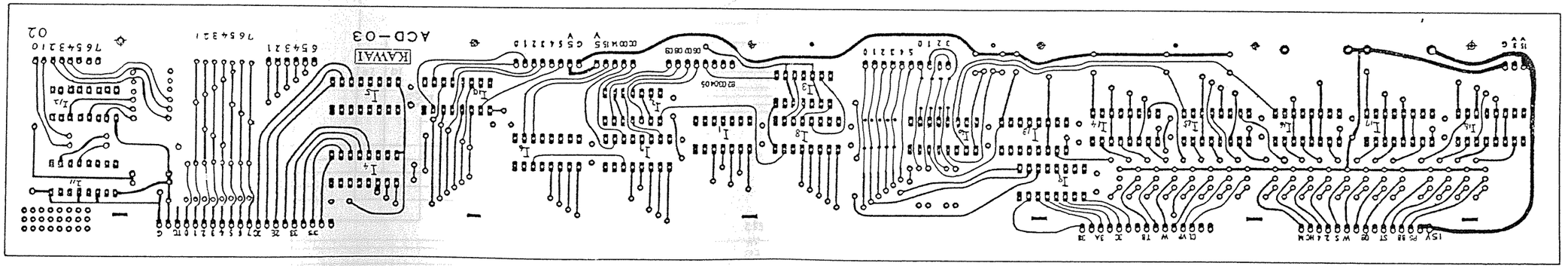
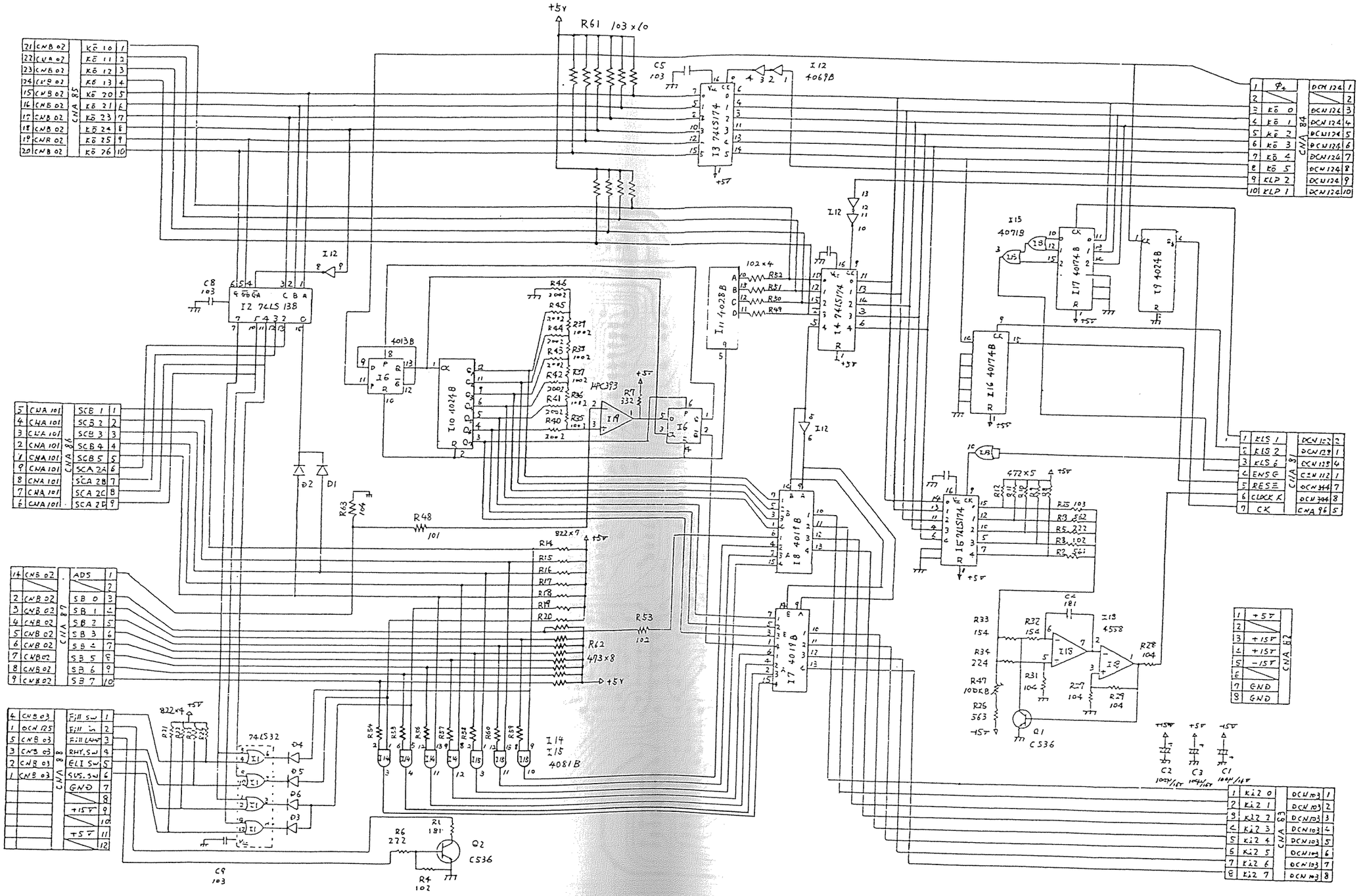
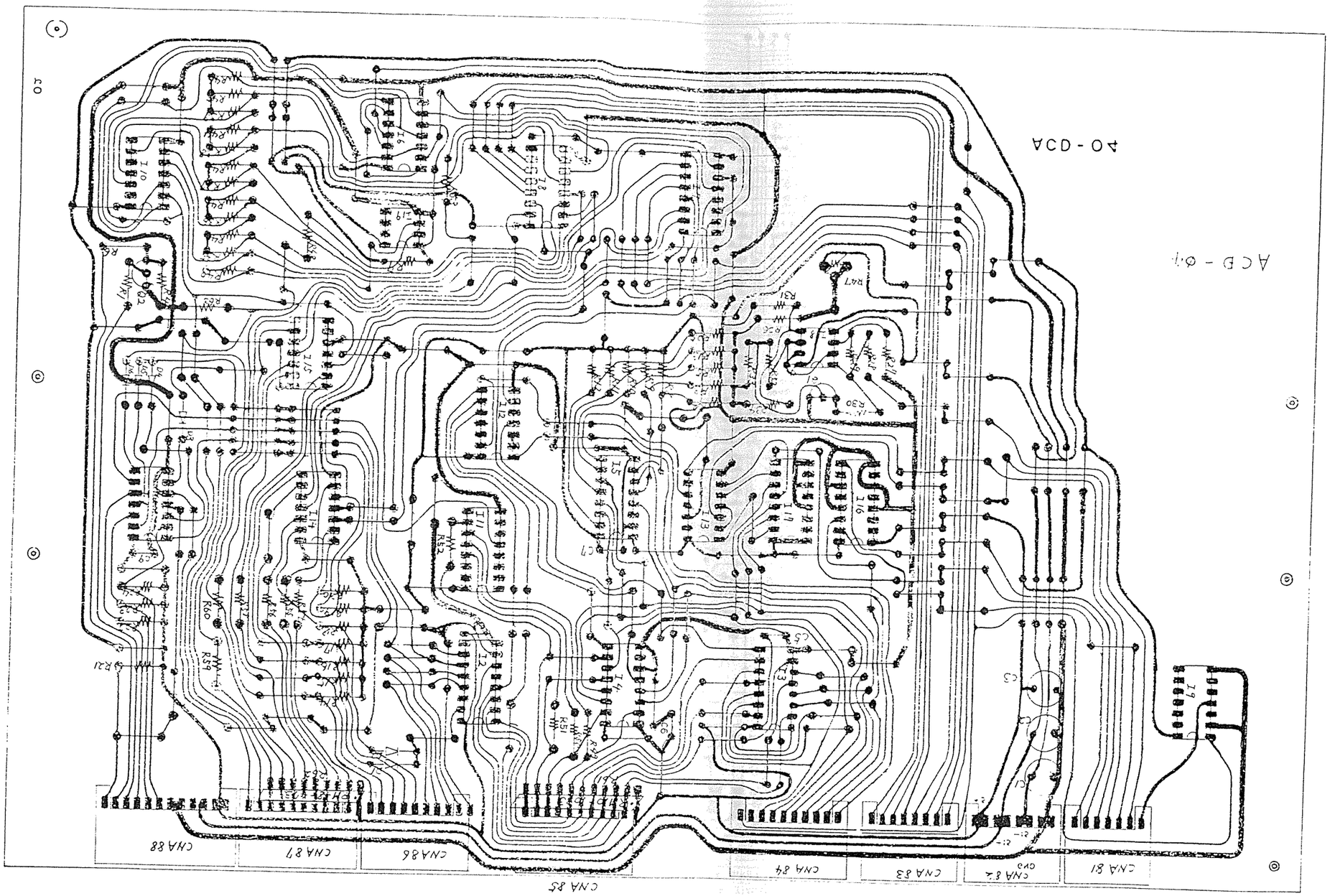
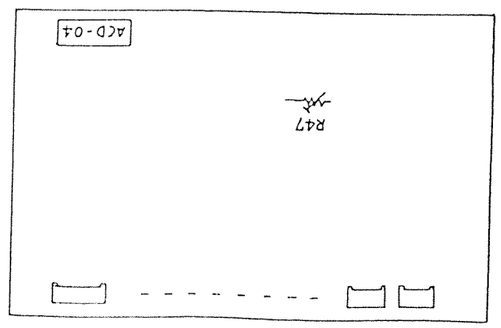
CNA72
CNA73
CNA74
CNA75
CNA76
CNA77
CNA78


ACD-03
KAWAI

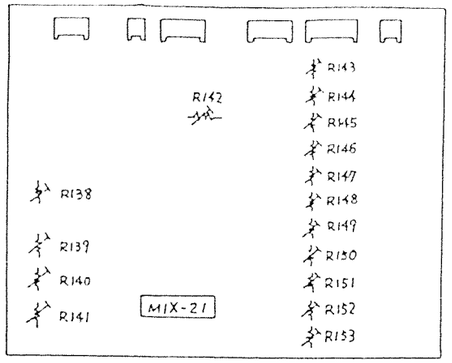
11. KEY SCANNING DECODE (for Box) < ACD-04 >



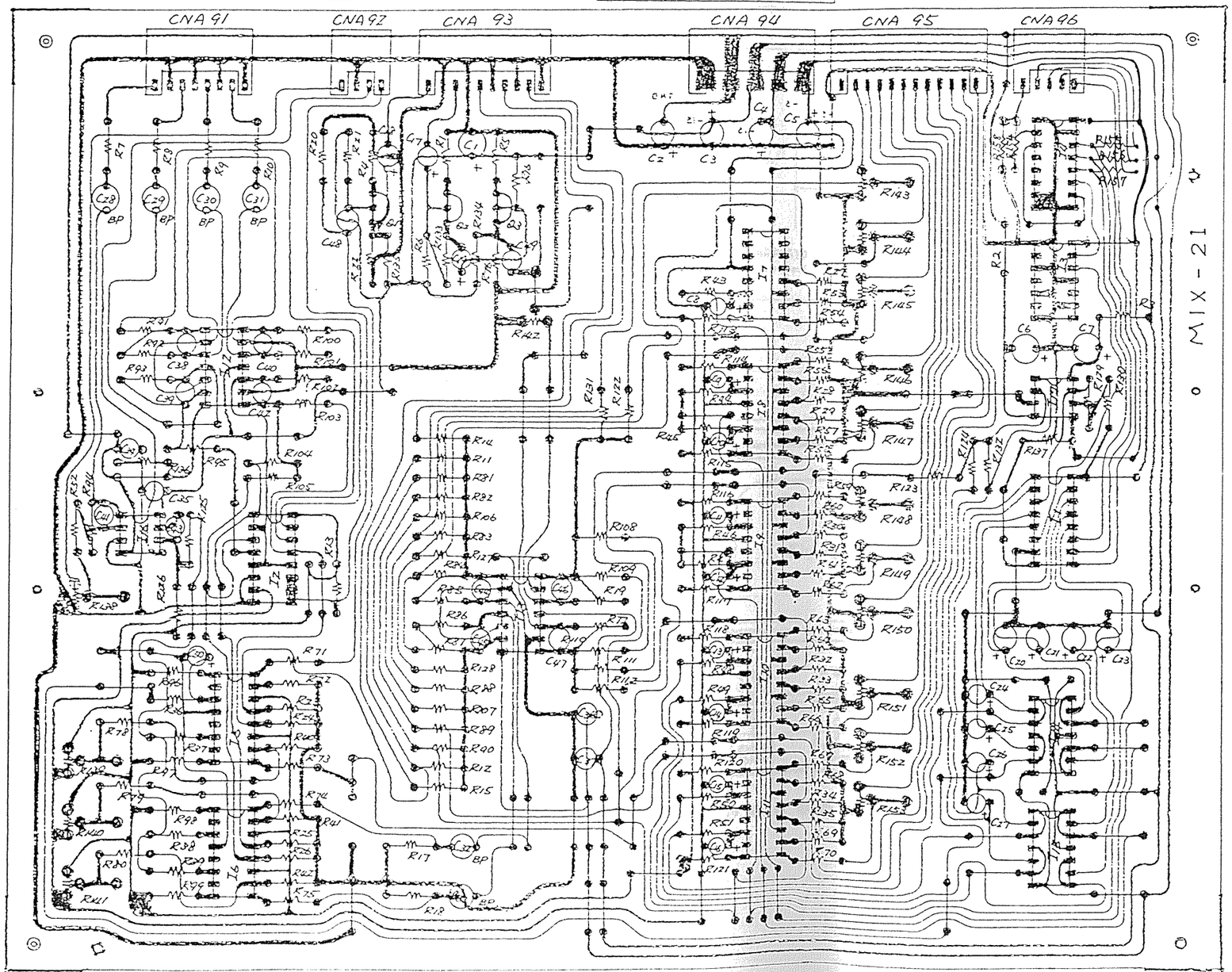




ACD 04	R47	LFO SPEED ADJ.

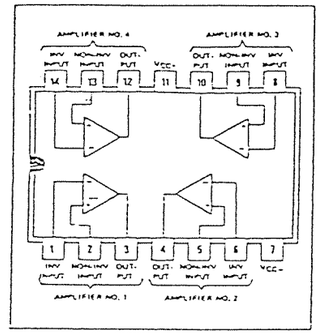


MIX-21	R 138	MIC VOLUME ADJ.
	R 139	FLUTE OFFSET ADJ.
	R 140	GEN(R) OFFSET ADJ.
	R 141	GEN(L) OFFSET ADJ.
	R 142	REV. VOLUME ADJ.
	R 143	ARP. VOLUME ADJ.
	R 144	ACC. VOLUME ADJ.
	R 145	RHY. VOLUME ADJ.
	R 146	BASS VOLUME ADJ.
	R 147	ENS. BASS VOLUME ADJ.
	R 148	CHO. STR. VOLUME ADJ.
	R 149	CHO. FLUTE VOLUME ADJ.
	R 150	TRE. STR. VOLUME ADJ.
	R 151	TRE. FLUTE VOLUME ADJ.
	R 152	P.PERCUS VOLUME ADJ.
	R 153	SYN.SOUND VOLUME ADJ.



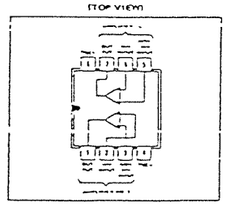
RC4136

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

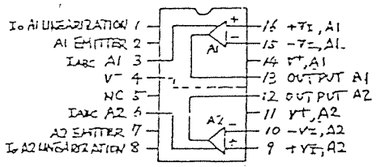


RC4558

(TOP VIEW)



CA3280G

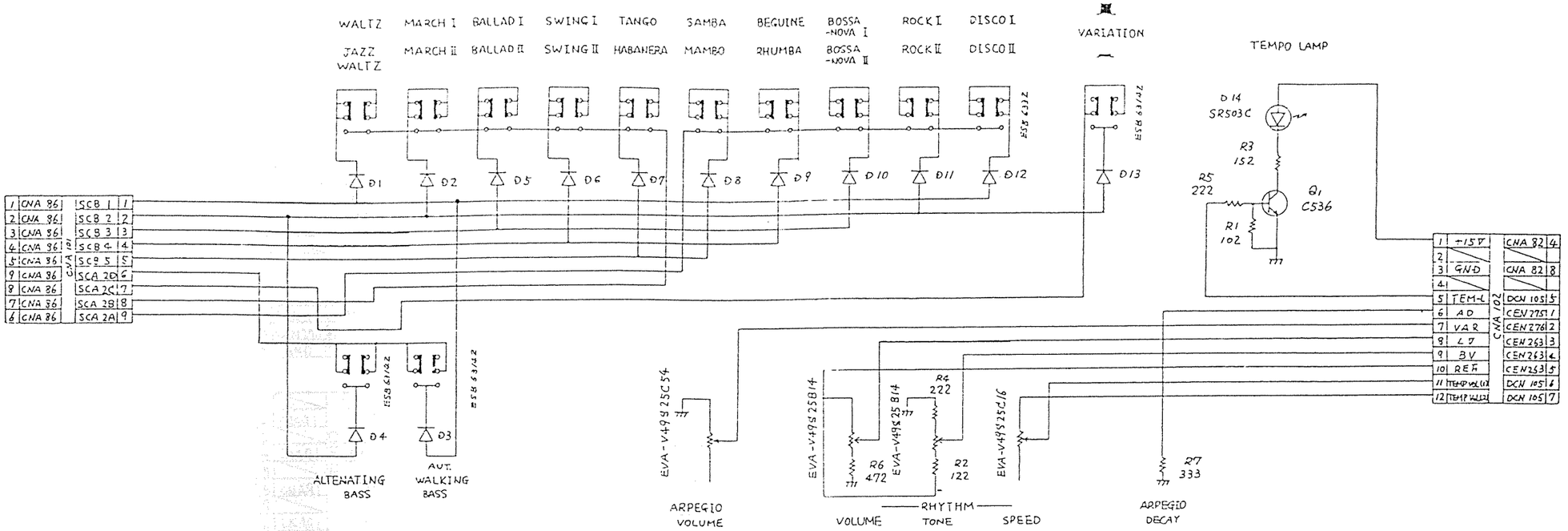


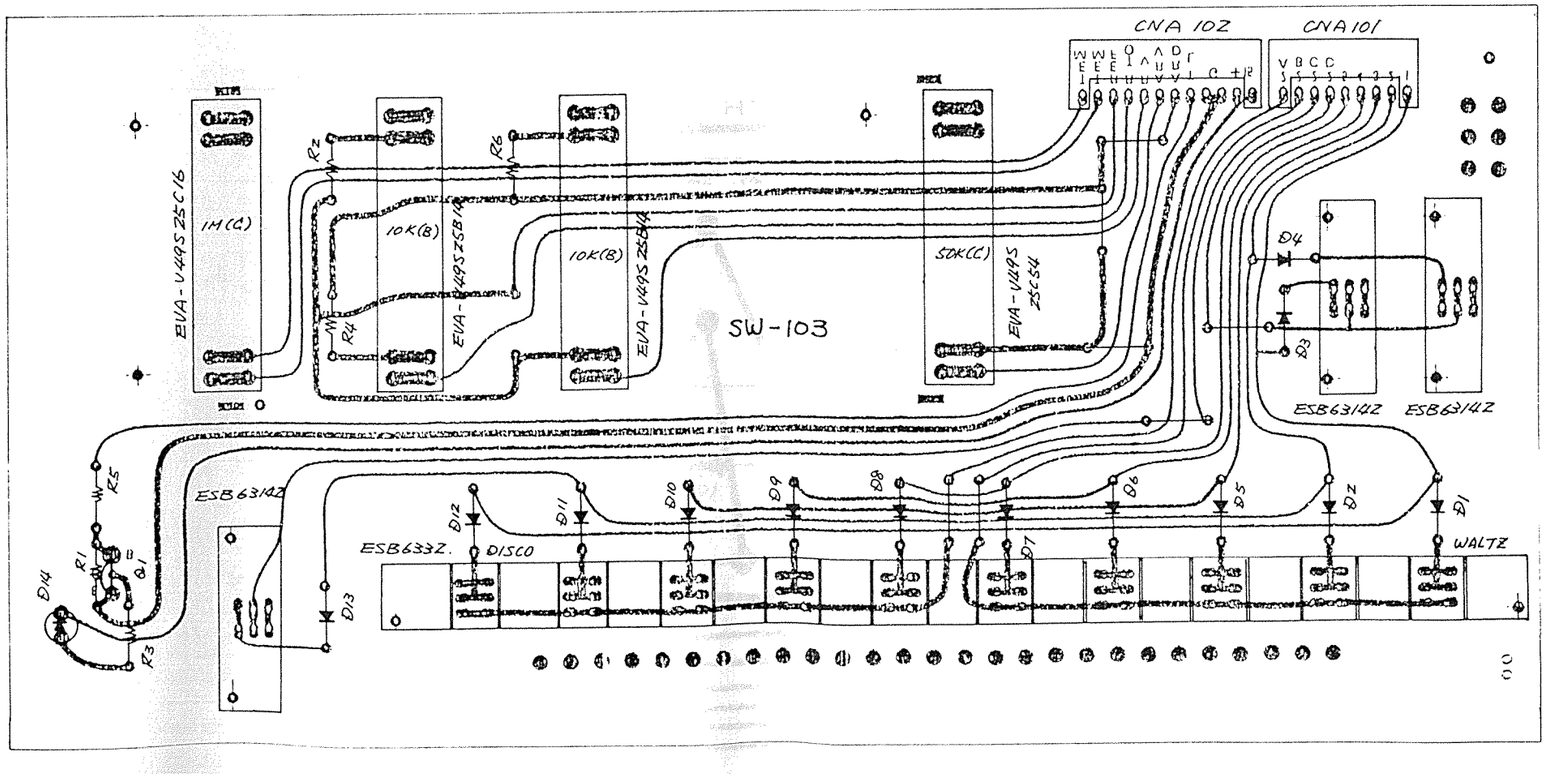
CD4520B

TRUTH TABLE

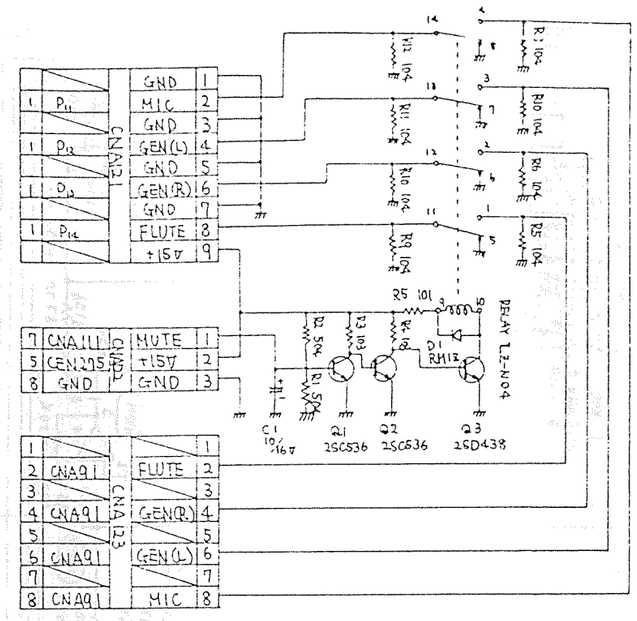
CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↓	0	No Change
↑	0	0	No Change
↓	0	0	No Change
1	↓	0	No Change
X	X	1	Q1 thru Q4 = 0

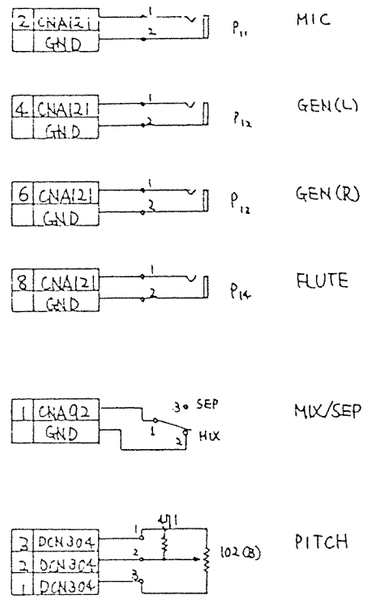
13. BOX PANEL CIRCUITS < SW-103 >

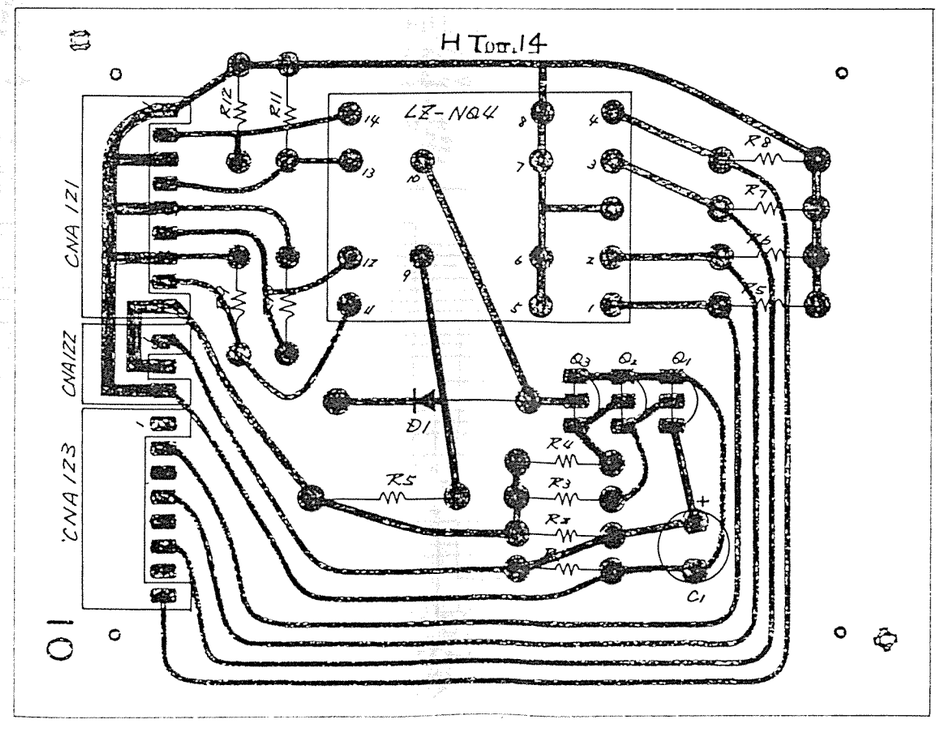




14. MUTING RELAY CIRCUIT < HT-14 >



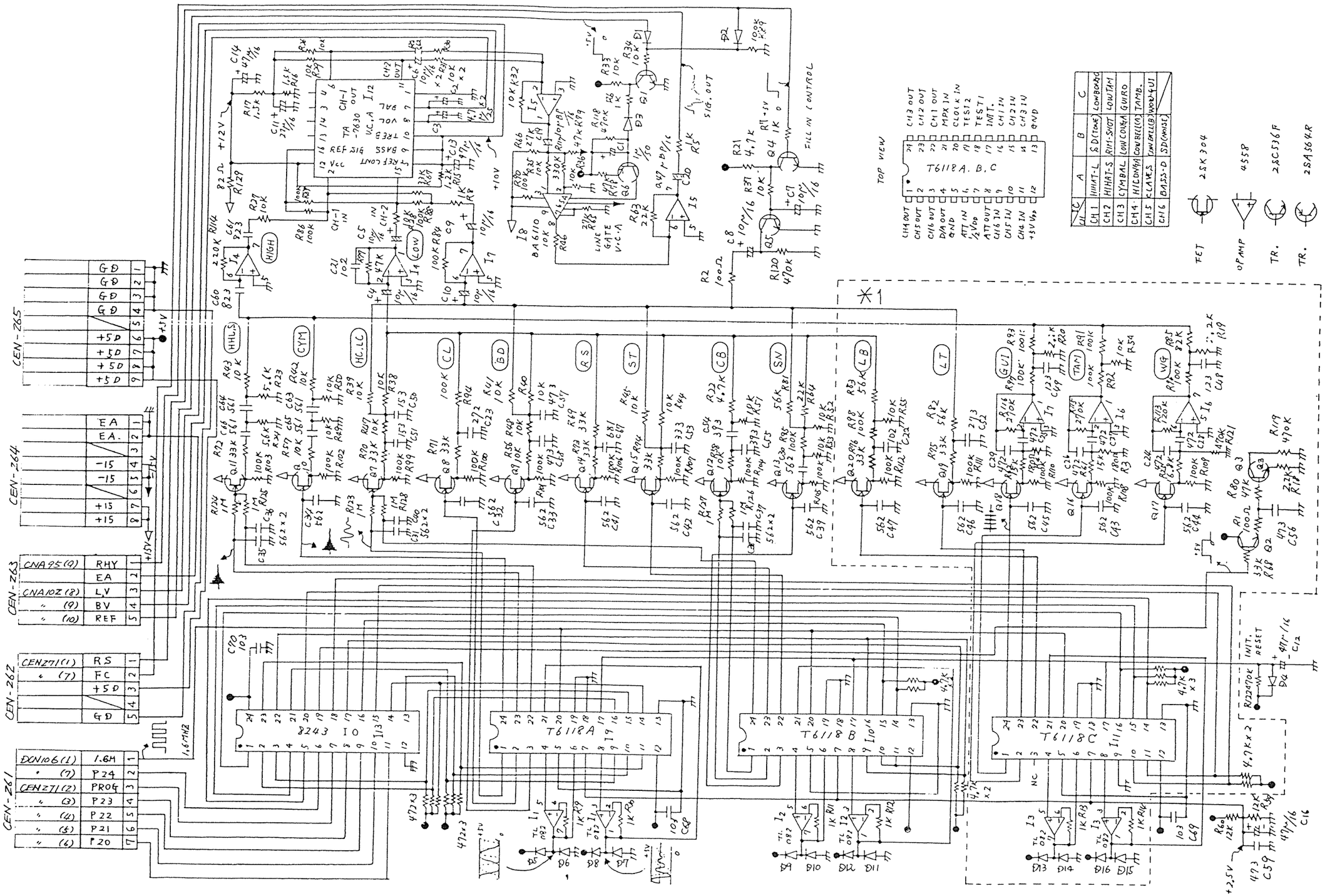


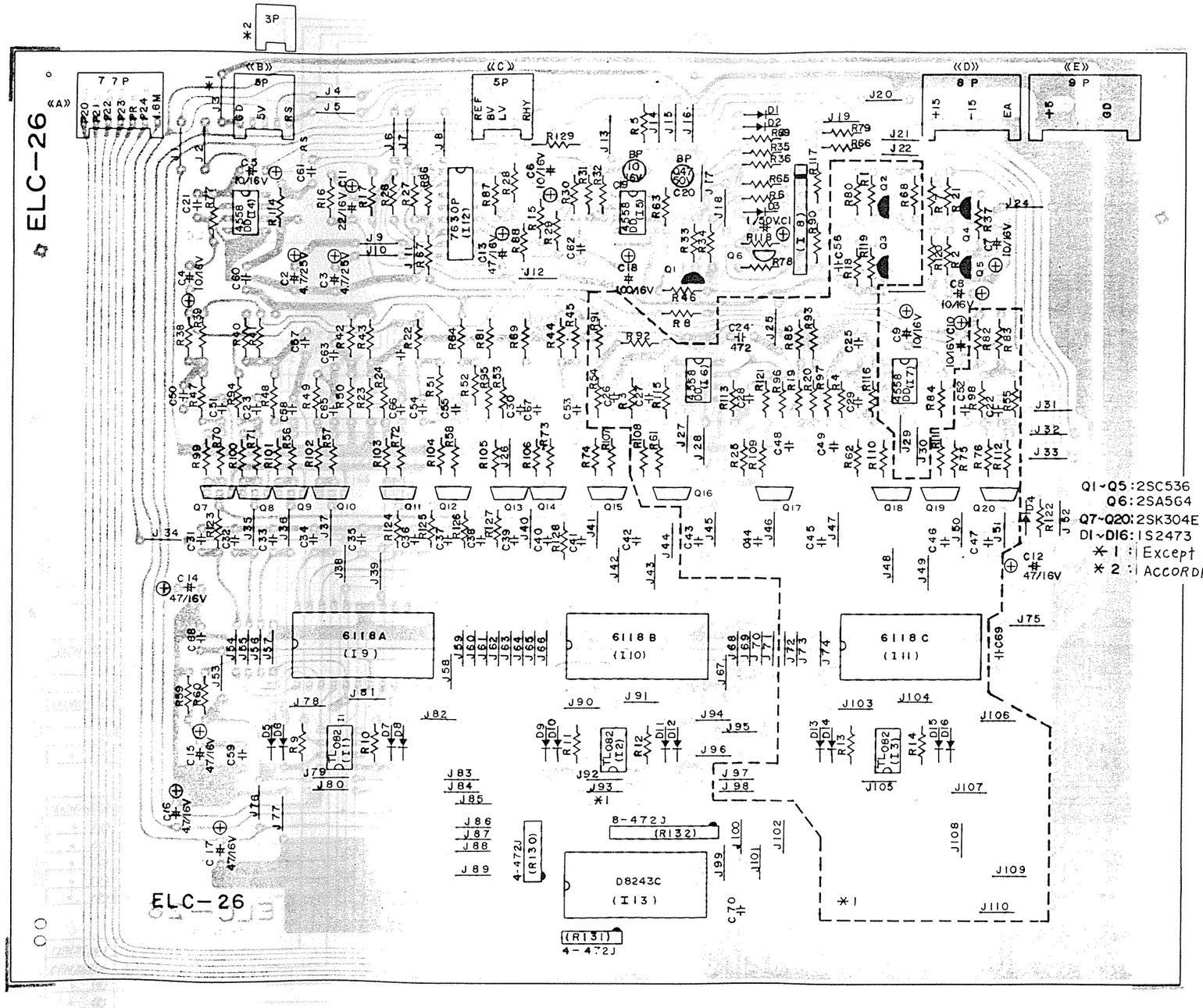


* 1 Not Use

15. RHYTHM TONE GENERATOR CIRCUITS

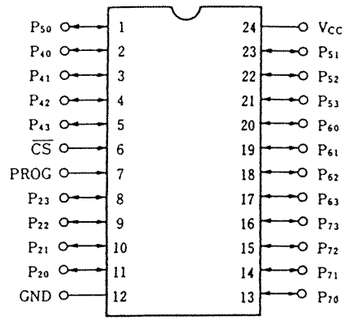
ELC-26 (1)





μPD8243C

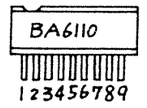
■ I/O Expander Port

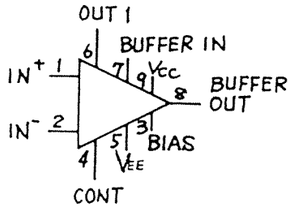


P_{20}~P_{23} : Input Output port (Port 2)
P_{40}~P_{43} : Input Output port (Port 4)
P_{50}~P_{53} : Input Output port (Port 5)
P_{60}~P_{63} : Input Output port (Port 6)
P_{70}~P_{73} : Input Output port (Port 7)
$\overline{CS}$: Chip Select
PROG : Program pulse

■ BA6110

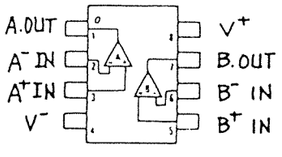
Voltage Controlled Amp.





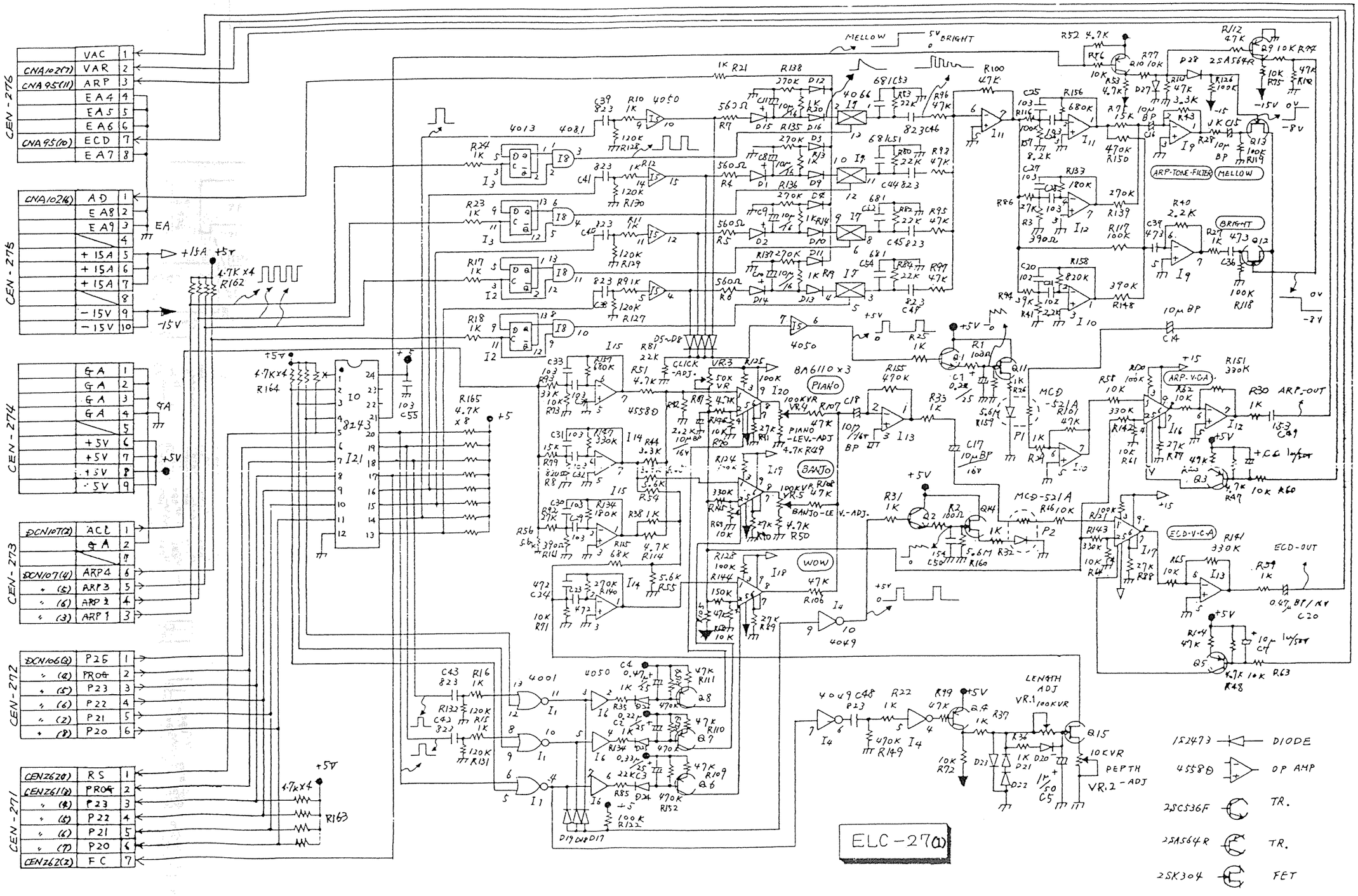
■ NJM4558DD

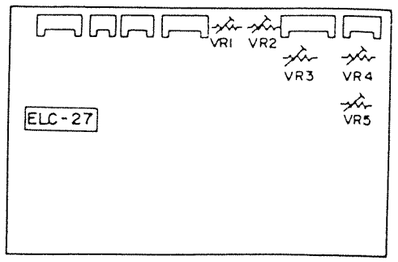
Dual OP-AMP



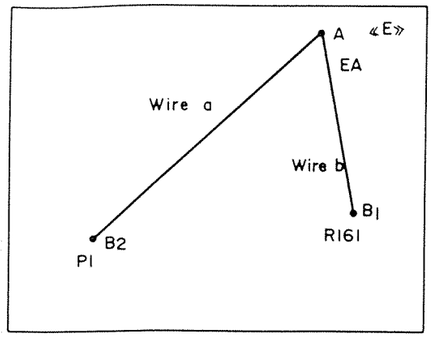
16. ELECTRO CHORD & AUTO ARPEGGIO CIRCUITS

ELC-27 (1)



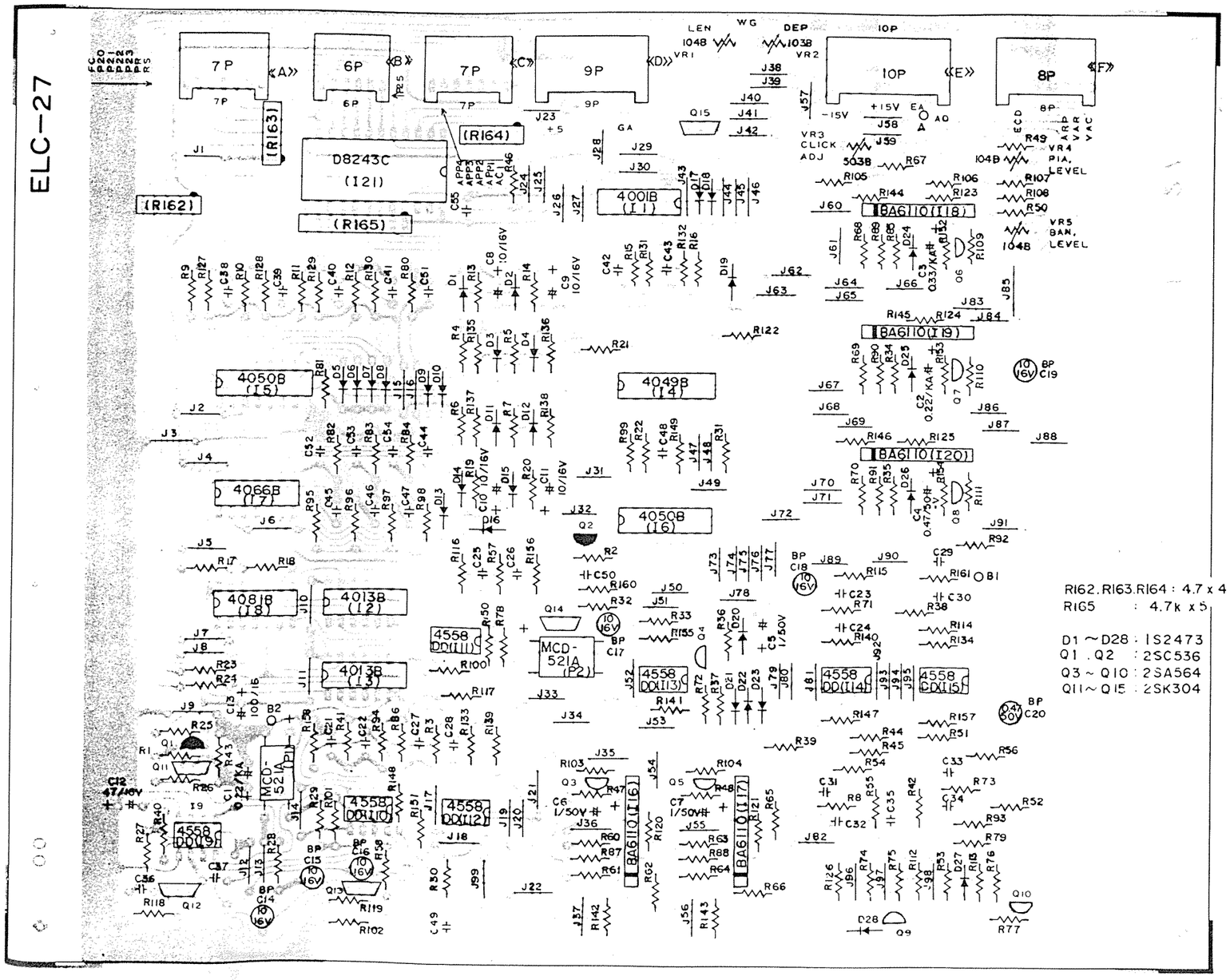


E	VR- 1	LENGTH ADJ. FOR WOW GUITAR
L	VR- 2	DEPTH ADJ. FOR WOW GUITAR
C	VR- 3	VCA OFFSET ADJ
I	VR- 4	PIANO VOLUME ADJ.
27	VR- 5	BANJO VOLUME ADJ.



R162 · R163 · R164 : 4.7 x 4
R165 : 4.7K x 5

D1 ~ D28 : 1S2473
Q1 · Q2 : 2SC536
Q3 ~ Q10 : 2SA564
Q11 ~ Q15 : 2SK304

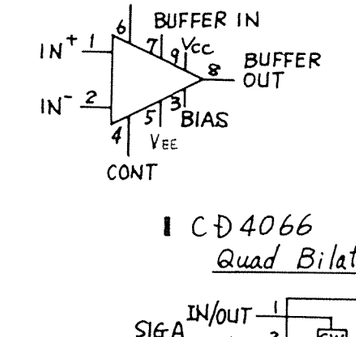


R162.R163.R164 : 4.7 x 4
R165 : 4.7k x 5

D1 ~ D28 : 1S2473
Q1 . Q2 : 2SC536
Q3 ~ Q10 : 2SA564
Q11 ~ Q15 : 2SK304

μPD8243C

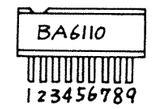
■ I/O Expander Port



P_{20} ~ P_{23} : Input Output port (Port 2)
P_{40} ~ P_{43} : Input Output port (Port 4)
P_{50} ~ P_{53} : Input Output port (Port 5)
P_{60} ~ P_{63} : Input Output port (Port 6)
P_{70} ~ P_{73} : Input Output port (Port 7)
$\overline{CS}$: Chip Select
PROG : Program pulse

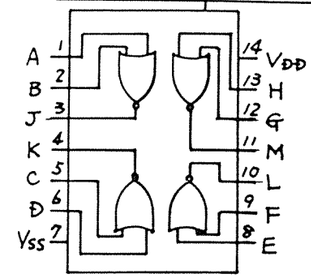
BA6110

Voltage Controlled Amp.



CD4001

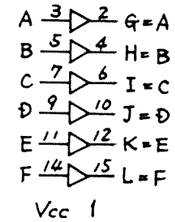
Quad 2-Input NOR Gate



Ex. $J = \overline{A+B}$

CD4050

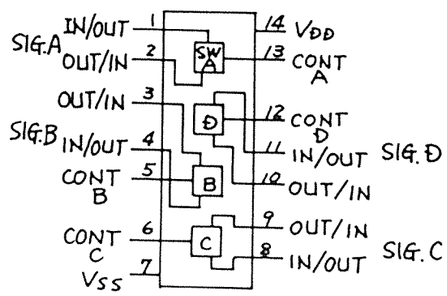
Hex Buffer/Converters



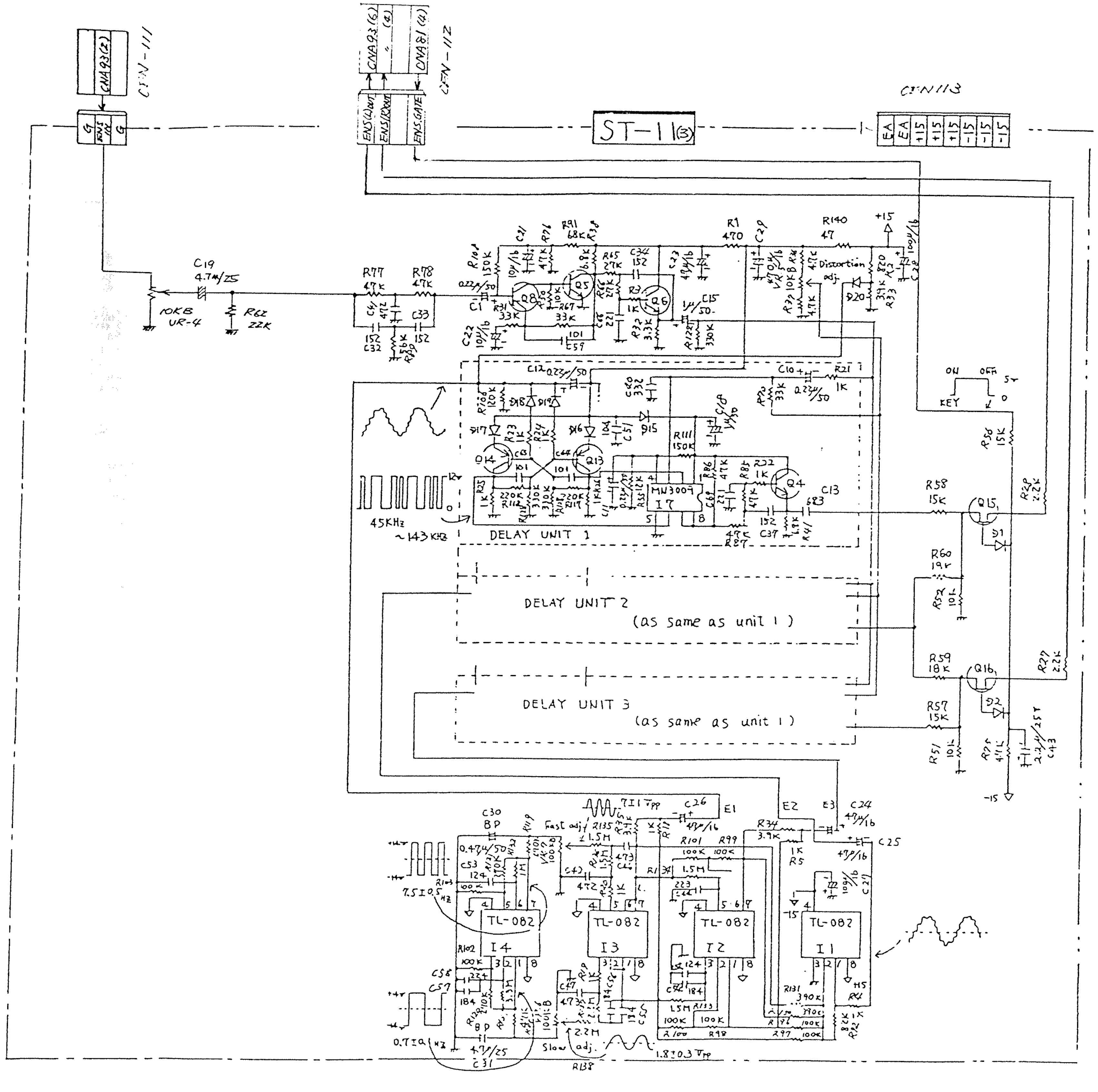
Vcc 1
Vss 8
NC 13,16

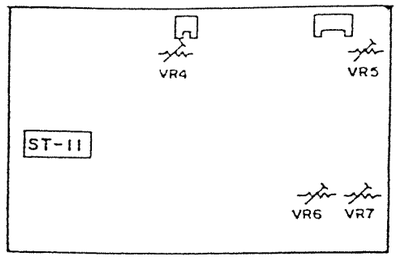
CD4066

Quad Bilateral Switch



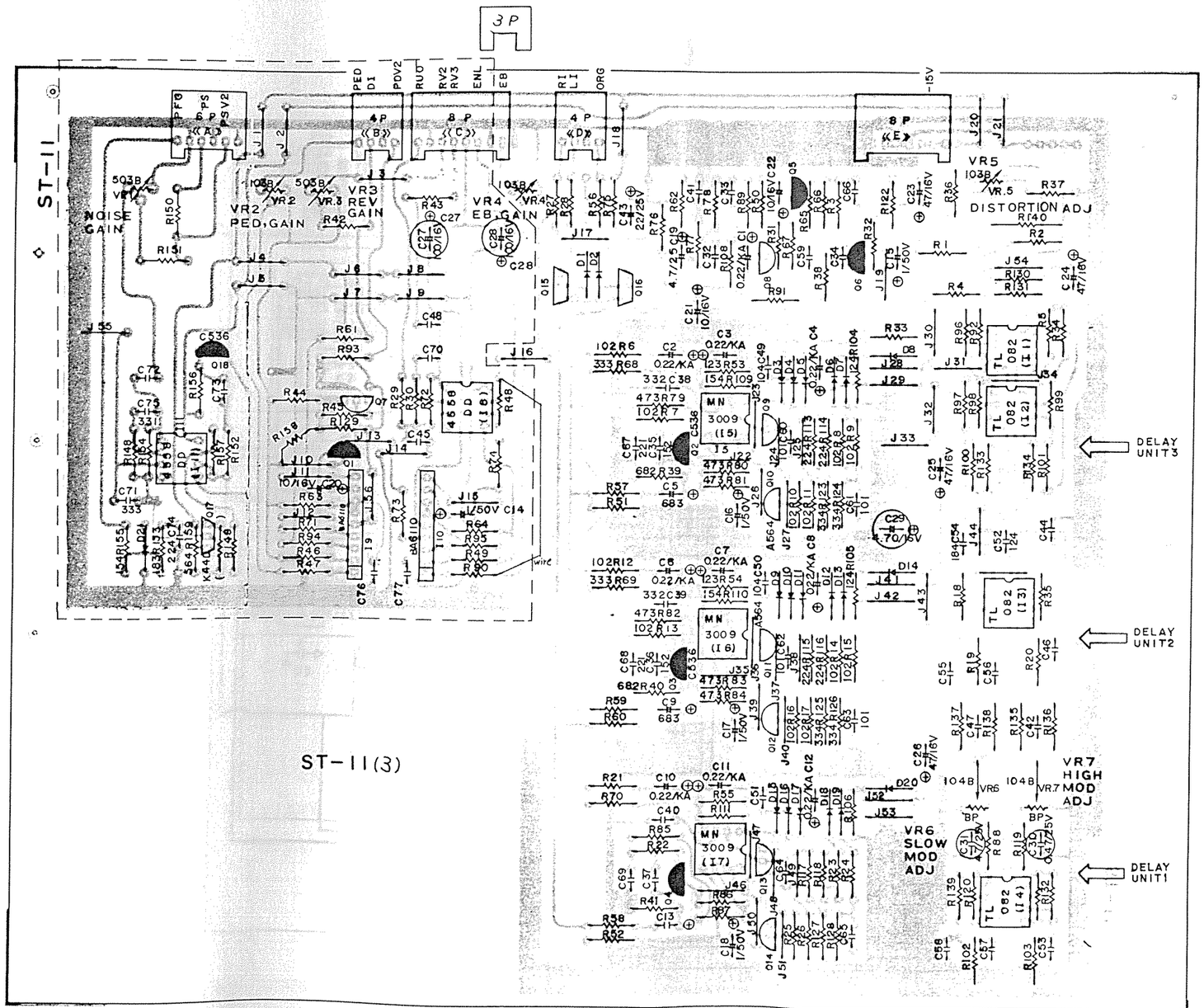
17. ENSEMBLE CIRCUITS
ST-11 (3)





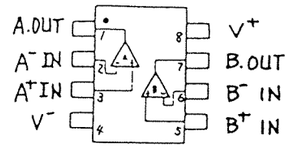
P.C.B.	VR. NO.	DESCRIPTION
ST-11	VR- 1	*1
	VR- 2	*1
	VR- 3	*1
	VR- 4	ENSEMBLE VOLUME ADJ.
	VR- 5	ENSEMBLE DISTORTION ADJ.
	VR- 6	SLOW MODURATION ADJ.
	VR- 7	FAST MODURATION ADJ.

*1 NOT USE

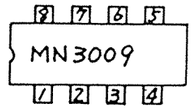


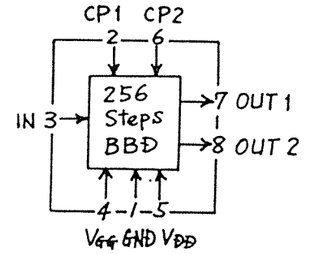
ST-11(3)

■ NJM4558DD
Dual OP-AMP

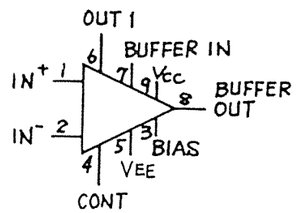


■ MN 3009
256 Steps BBD

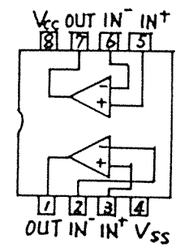




■ BA6110
Voltage Controlled Amp.



■ TL082CP
JET-INPUT OP-AMP



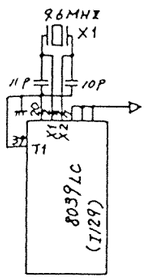
* : Capacitance 103

*8: MB8364 (Mask-ROM (1P21)) Pin Compatible

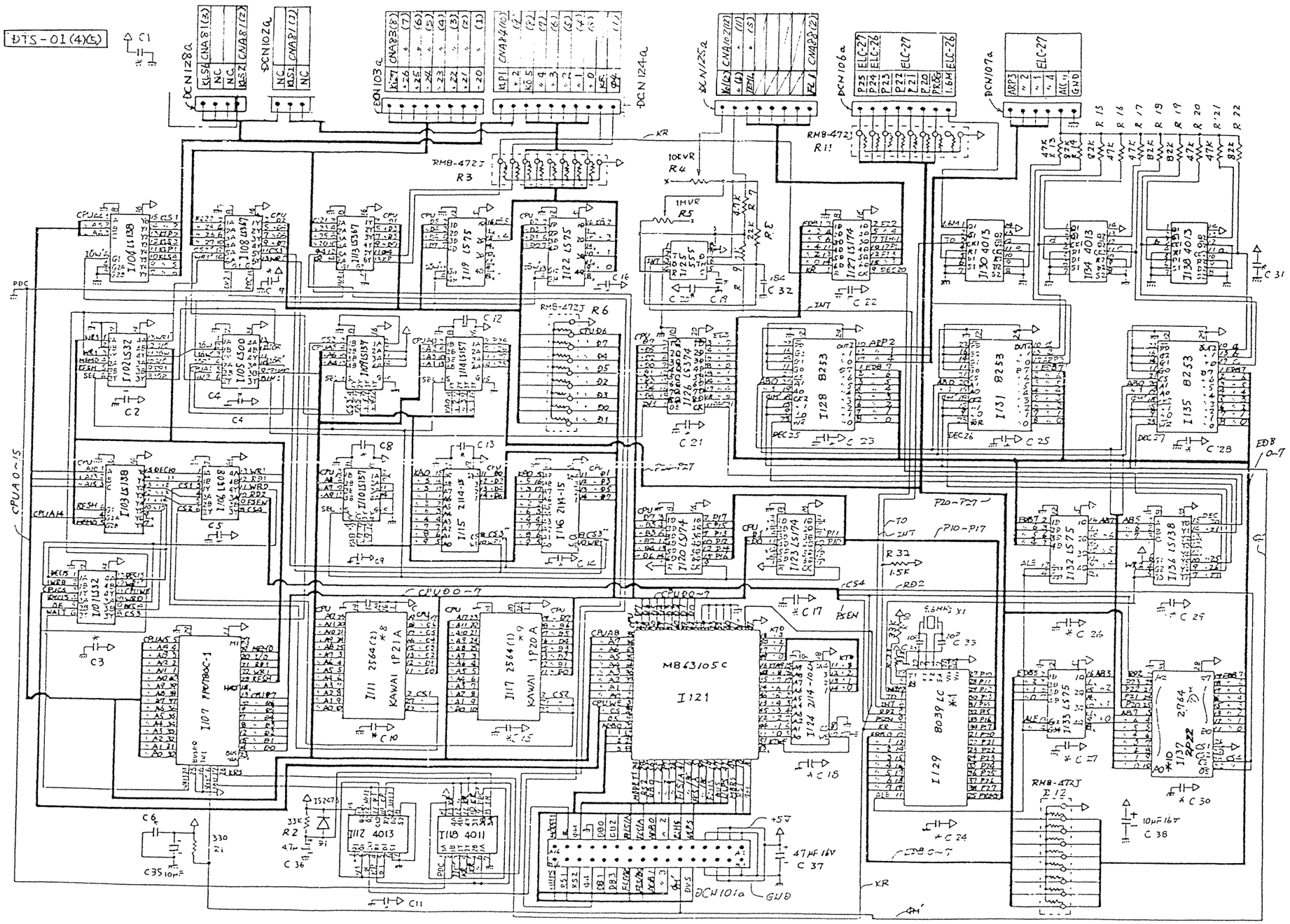
*9: MB8364 (Mask-ROM (1P20)) Pin Compatible
··· Except Canada, U.S.A Markets
U.S.A., Canada Markets ··· TM2564 (EP-ROM (2P24)) Pin Compatible

*10: TMM-2364P (Mask-ROM (2P22)) Pin Compatible

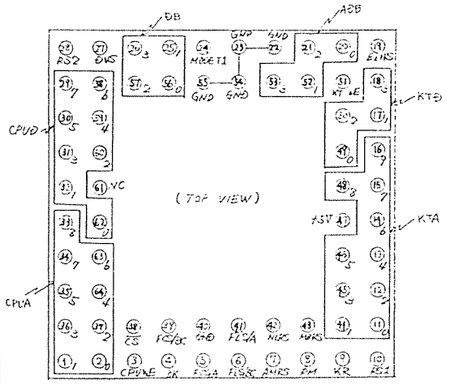
*1: In Case of Accordion, Show below



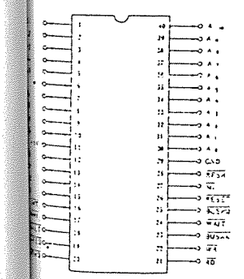
DTS-01(4)(5)

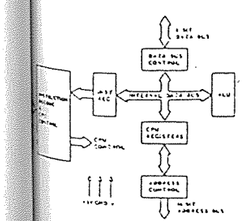


1 MB63105C
LSI for TC-1 Circuits

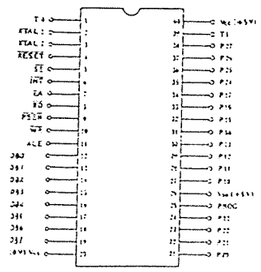


PD780C-1
8-Bit Microprocessors
Z80/Z80A-CPU Compatible

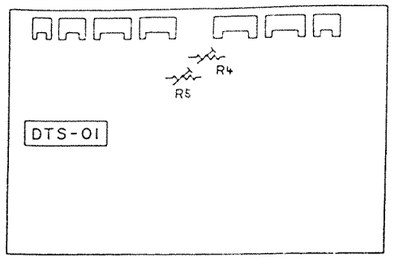




1 μPD 8039LC
1-Chip 8-Bit Microcomputer



P_{10}~P_{17} : I/O PORT (PORT 1)
P_{20}~P_{27} : 〃 (PORT 2)
DB_0~DB_7 : Data Bus
T_0, T_1 : Test
$\overline{INT}$: Interrupt
$\overline{RD}$: Read
$\overline{WR}$: Write
ALE : Address Latch Enable
$\overline{PSEN}$: Program Store Enable
$\overline{SS}$: Single Step
EA : External Access
XTAL 1, 2 : Crystal Input

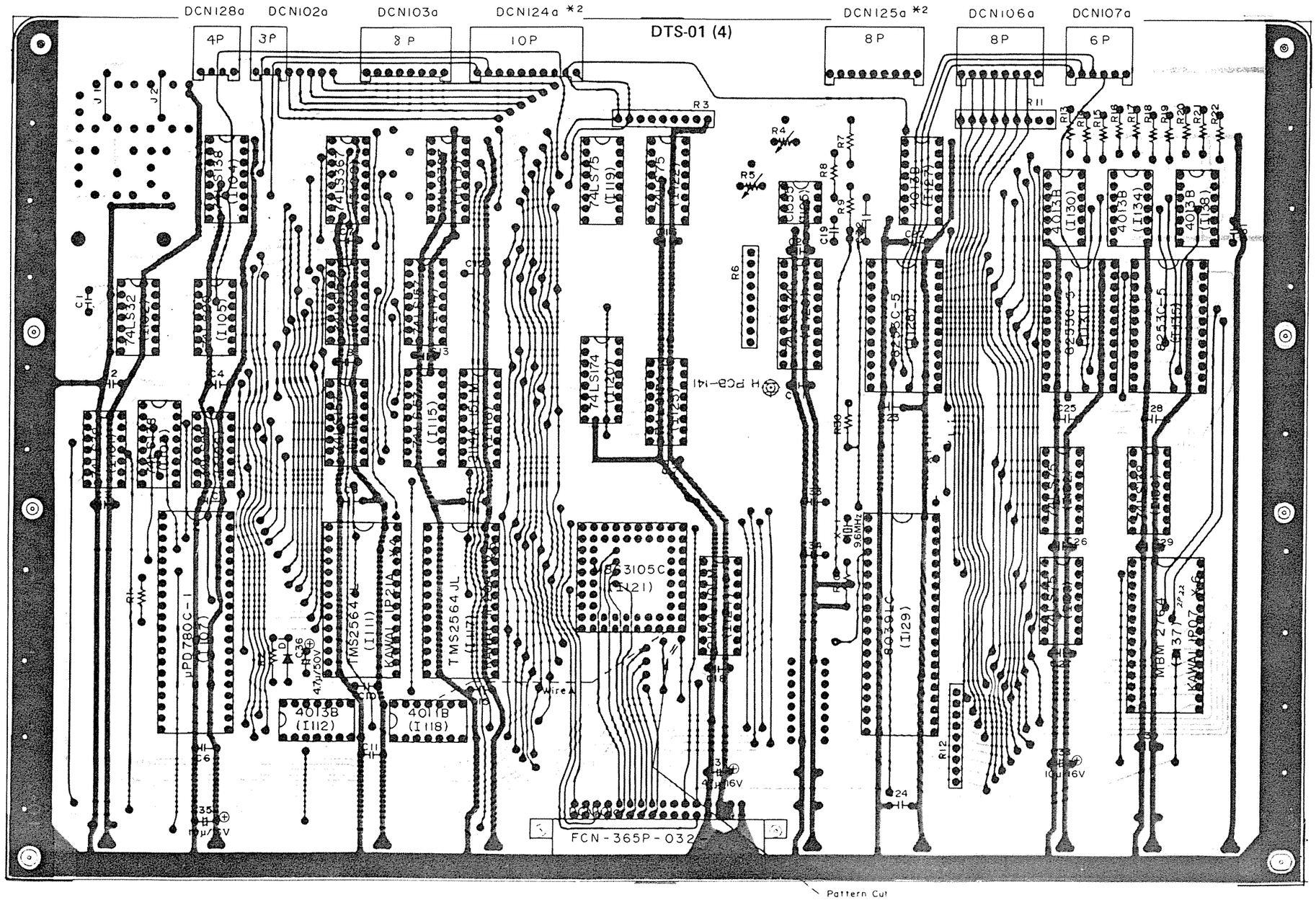


D T S 01	R-5	RHYTHM TEMPO ADJ. OF SLOW
	R-4	RHYTHM TEMPO ADJ. OF FAST

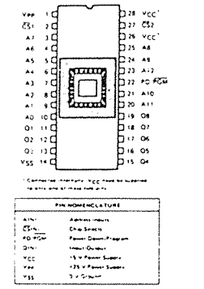
D1 1S2473

*4 MB8364 (Mask-ROM (1P21)) Pin Compatible
*5 MB8364 (Mask-ROM (1P20)) Pin Compatible
— Except Canada, U.S.A. Markets
Canada, U.S.A. Markets — TM2564 (EP-ROM (2P24)) Pin Compatible
*6 TMM-2364P (Mask-ROM (2P22)) Pin Compatible

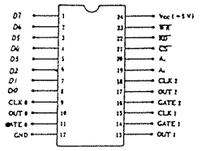
DCN128a DCN102a DCN103a DCN124a *2 DCN125a *2 DCN106a DCN107a



■ TMS 2564
64 K Bit Erasable Programmable ROM

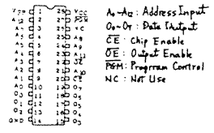


■ μPD 8253C-5
Programmable Interval Timer

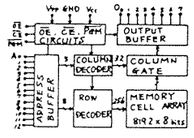


D0~D7 : Data Bus
CLK N : Counter Clock Inputs
GATE N : Counter Gate Inputs
OUT N : Counter Outputs
$\overline{RD}$: Read Counter
$\overline{WR}$: Write Command or Data
$\overline{CS}$: Chip, Select
A0·A1 : Counter Select

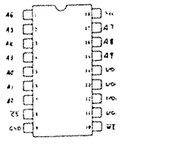
■ TMM 2764
64 K Bit EP ROM
MBM 2764 PIN Compatible
MASK ROM TMM 2364P PIN Compatible

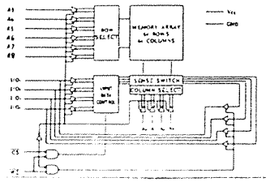


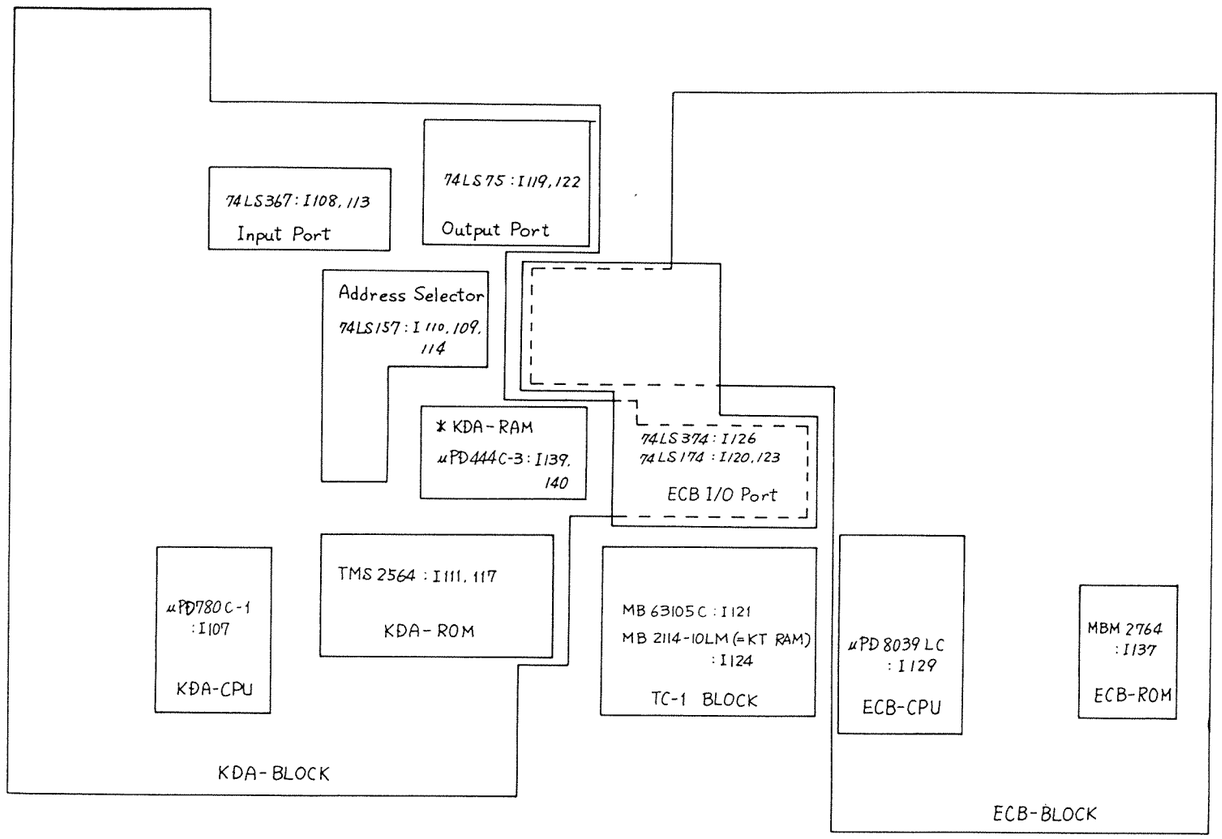
A0~A12 : Address Input
O0~O7 : Data Output
$\overline{CE}$: Chip Enable
$\overline{OE}$: Output Enable
$\overline{PGM}$: Program Control
NC : Not Use



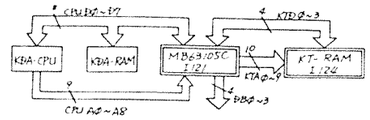
■ μPD 444C · MBM 2114A-10L/15L
4096 Bit Static CMOS RAM





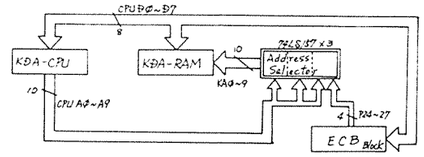


■ **TC-1 Block**



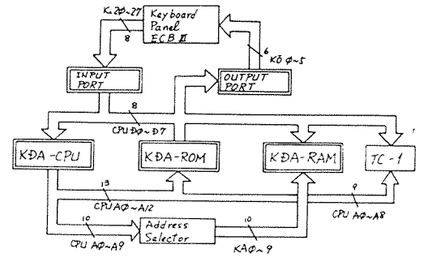
Data of KDA-RAM is sent to I 121. Data Signal (=DBϕ ~ 3), which is desired for final calculation in each block of ADSR · FNG · HCC · WFG, is distributed through KT-RAM (I 124).
Timing Signal (=KTAϕ ~ 9) for data-distribution is emitted from I 121.

■ **Address Selector Block**



Since KDA-RAM is availed for temporarily housing data of Manual-, Pedal-relationship and automatic accompaniment (E.C.B. III) function, selection of data is performed in this block.
Control Signal (=SEL) for selection is made by using KDA-CPU's Signal (=MEMO̅, RFSH).

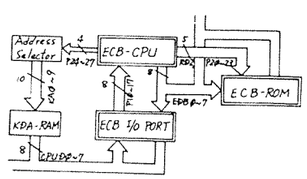
■ **KDA-CPU · KDA-ROM · KDA-RAM · INPUT PORT · OUTPUT PORT BLOCK**



KDA-ROM indicates KDA-CPU to output signals which are scanning the keyboard, PANEL and E.C.B. III sections. Then scanning pulse is output to the keyboard, PANEL and E.C.B. III section through OUTPUT PORT from KDA-CPU immediately.
Condition data of these parts is put in to KDA-CPU through INPUT PORT.
Data *1 (this is memorized in KDA-ROM in advance) relating to the signal that has a change of condition is written in KDA-RAM by indication of KDA-CPU.

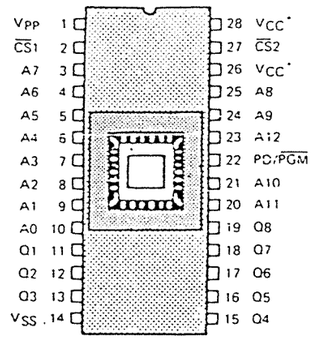
*1:
- Keyboard assignment (U: 8ch, L: 7ch, P: 1ch)
- Data to decide the priority of tone and to select the effect of tone to be added
- Content of organ preset
- Data to an envelope
- Data to be used in Sound System Block

■ **ECB-CPU · ECB-ROM · ECB I/O PORT Block**



ECB-CPU takes in necessary data (ex. Lower, Pedal key data and condition data of Arp. or Acc.: CPUDϕ ~ 7) out of the data housed in KDA-RAM through ECB I/O Port.
Dealing is performed on the basis of these data according to what ECB-ROM provides. ECB-ROM memorized in advance the pronouncing timing of Arp. Pattern or Acc. Pattern and outputs necessary data in accordance with Address Signal (=P2ϕ ~ 23, RD2, EDBϕ ~ 7) coming from ECB-CPU.
In turn, ECB-CPU puts in this data and outputs it to the circuit (ELC-26, 27, 40, 41) for automatic accomapniment (E.C.B. III).

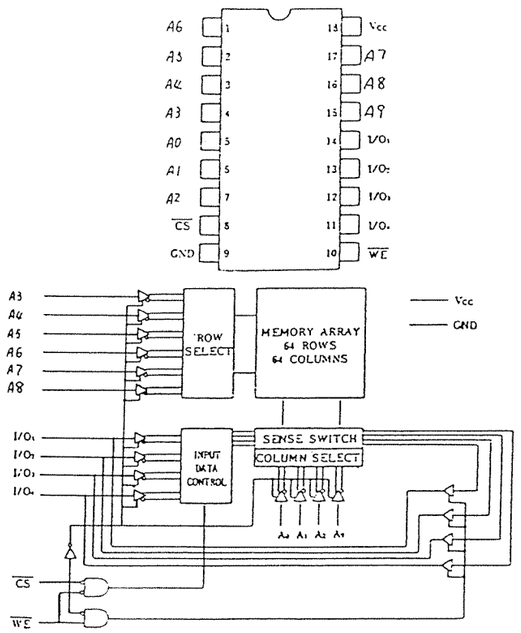
TMS 2564
64 K Bit Erasable Programmable ROM



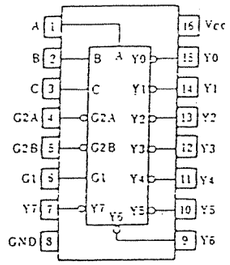
* Connected internally, V_{CC} need be supplied to only one of these two pins.

PIN NOMENCLATURE	
A(N)	Address inputs
$\overline{CS}$(N)	Chip Selects
PD/PGM	Power Down/Program
O(N)	Input/Output
V_{CC}	+5 V Power Supply
V_{PP}	+25 V Power Supply
V_{SS}	0 V Ground

μPD 444C · MBM 2114A-10L/15L
4096 Bit Static CMOS RAM

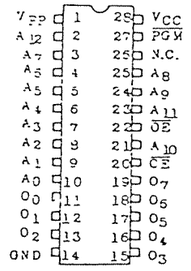


MB 74LS138
3-Line to 8-Line Decoder/Demultiplexer

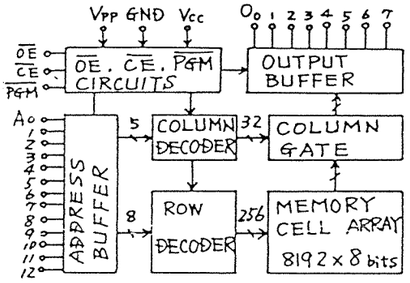


INPUT					OUTPUT							
ENABLE		SELECT										
G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
×	H	×	×	×	H	H	H	H	H	H	H	H
L	×	×	×	×	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

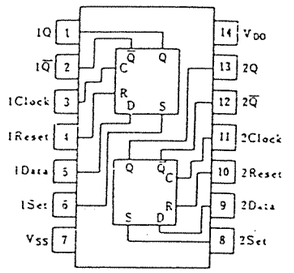
TMM 2764
64 K Bit EP ROM
MBM 2764 : PIN Compatible
MASK ROM TMM 2364P : PIN Compatible



A_0~A_{12} : Address Input
O_0~O_7 : Data Output
$\overline{CE}$: Chip Enable
$\overline{OE}$: Output Enable
$\overline{PGM}$: Program Control
NC : Not Use



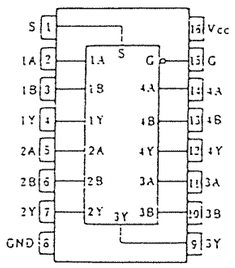
MB 84013B
Dual D-Type Master Slave Flip-Flop
CD 4013 : PIN Compatible



INPUT				OUTPUT	
Clock	Data	Reset	Set	Q	Q̄
↑	0	0	0	0	1
↑	1	0	0	1	0
↓	×	0	0	Q*	Q̄*
×	×	1	0	0	1
×	×	0	1	1	0
×	×	1	1	1	1

*: No Change

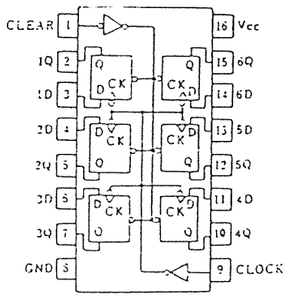
MB74LS157
Quadruple 2-Line to 1-Line Data Selector/ Multiplexer



INPUT				OUTPUT
G	S	A	B	Y
H	×	×	×	L
L	L	L	×	L
L	L	H	×	H
L	H	×	L	L
L	H	×	H	H

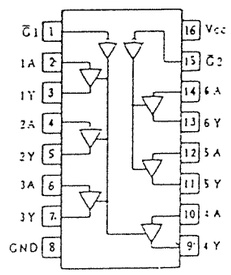
G : Strobe
S : Select

MB74LS174
Hex D-Type Flip-Flop with Common Direct Clear



INPUT			OUTPUT
CLEAR	CLOCK	D	Q
L	×	×	L
H	↑	H	H
H	↑	L	L
H	L	×	Q_0

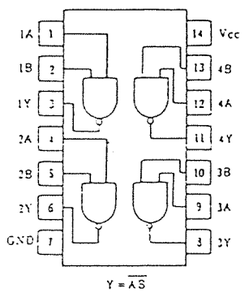
MB74LS367
Hex Bus Driver



INPUT		OUTPUT
G	A	Y
H	×	Z
L	L	L
L	H	H

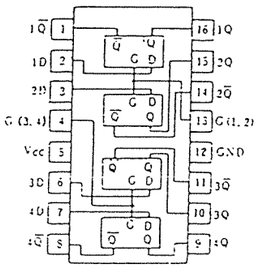
Z : High Impedance

MB74LS00
Quadruple 2-Input Positive-NAND Gate



$Y = \overline{AS}$

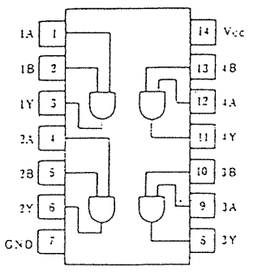
MB74LS75
4-Bit Bistable Latch



INPUT		OUTPUT	
D	G	Q	Q̄
L	H	L	H
H	H	H	L
×	L	Q_0	$\overline{Q_0}$

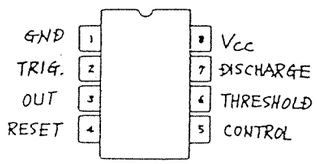
G : ENABLE

MB 74LS 08
Quadruple 2-Input Positive-AND Gate

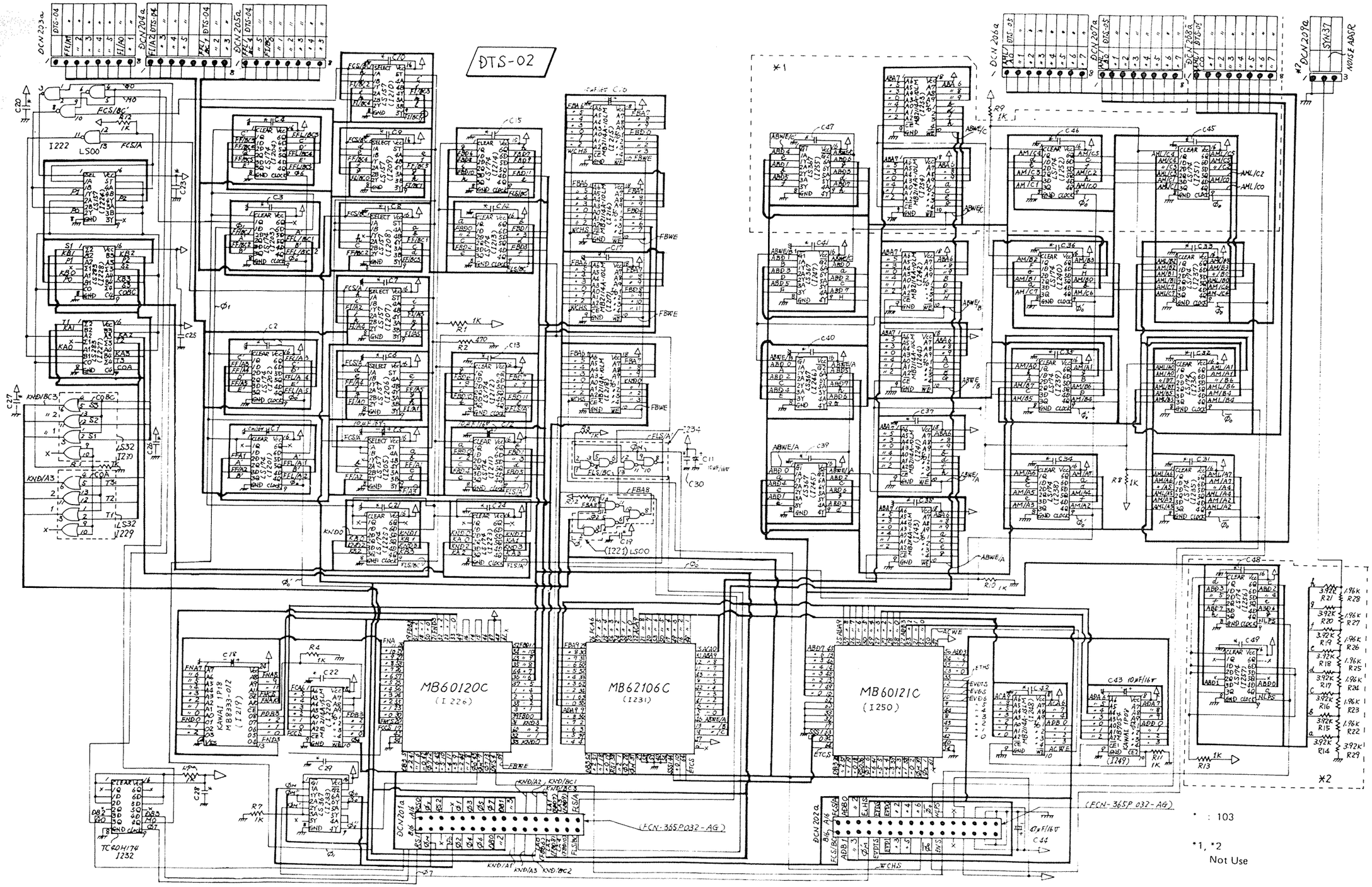


$Y = AB$

C 1555
Timer

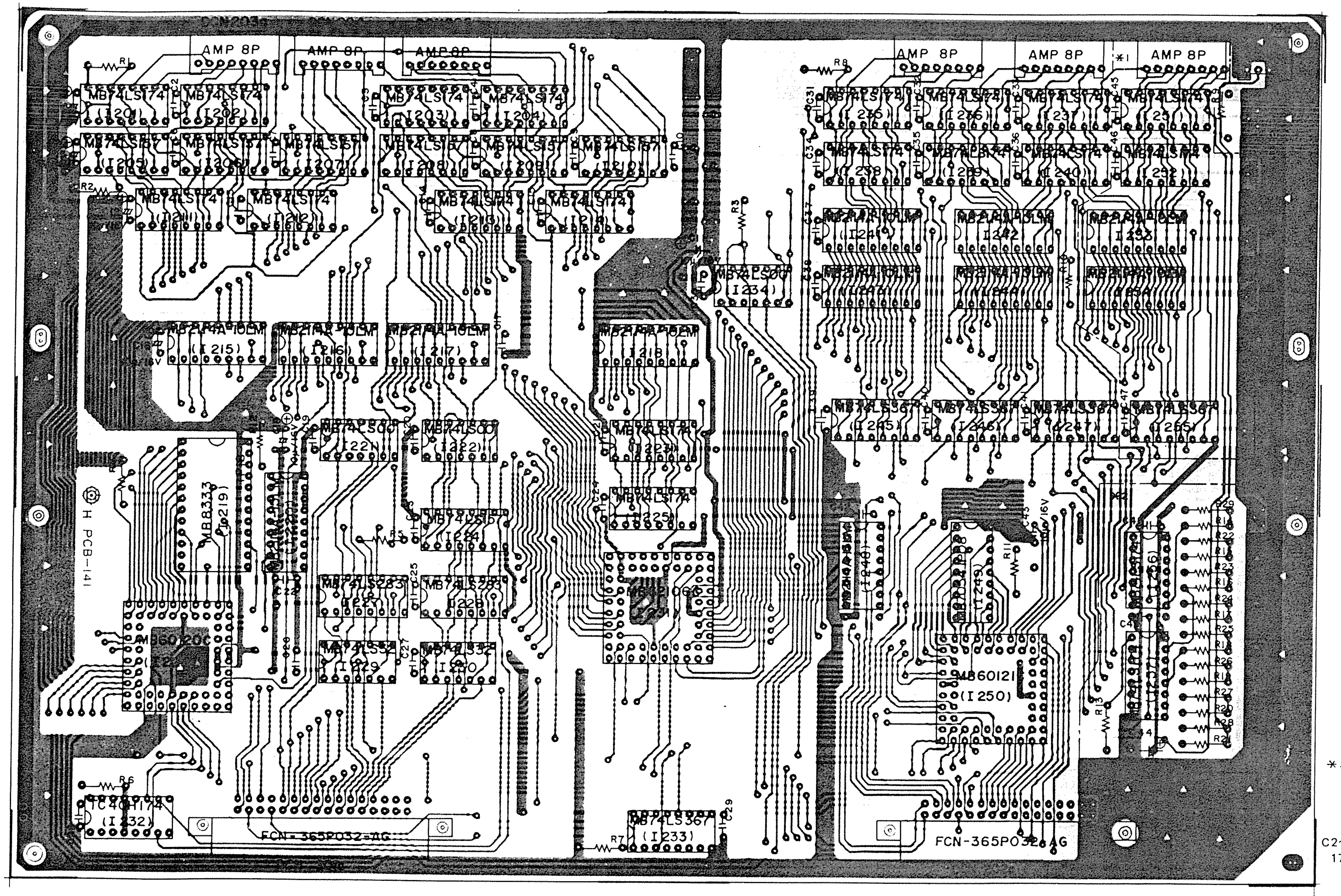


19. TC · ADSR · FNG CIRCUITS
DTS-02 (1)



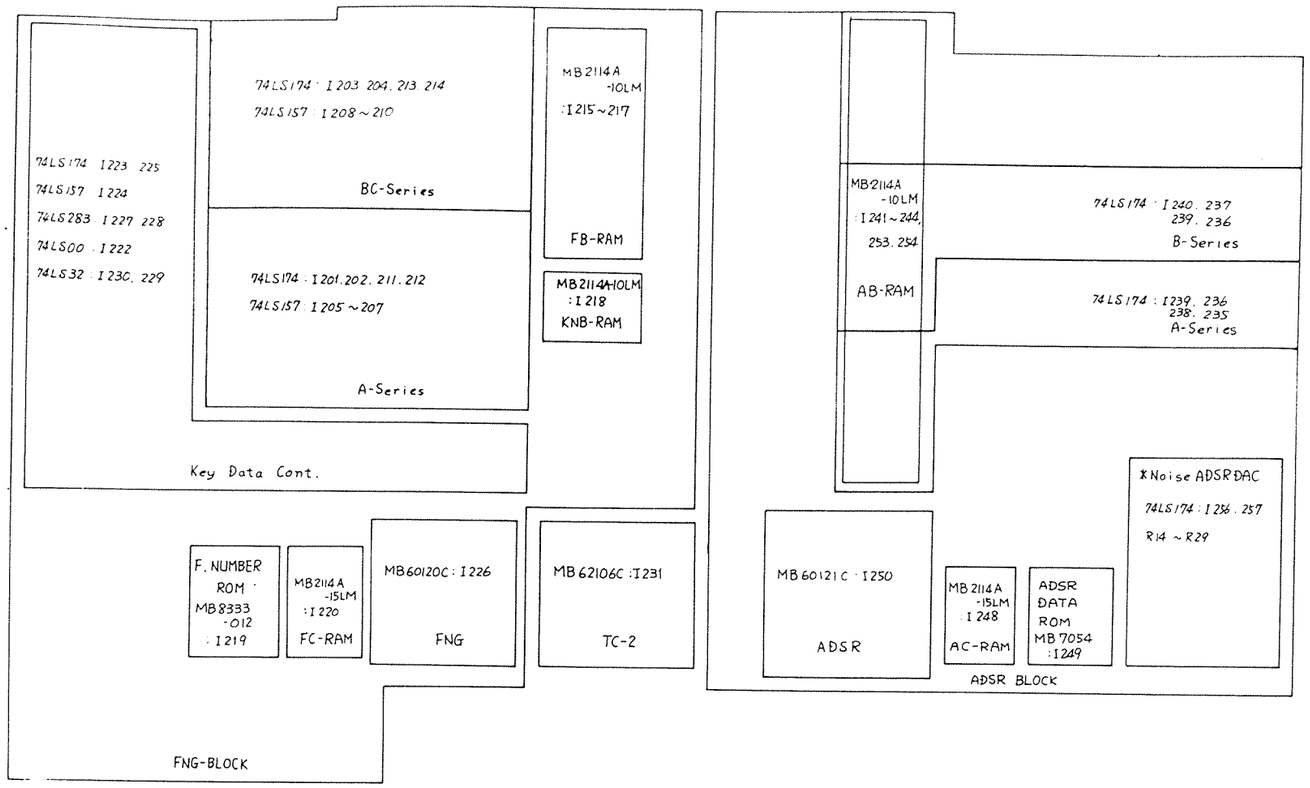
* : 103

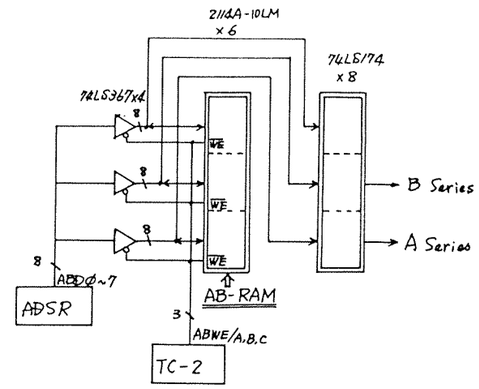
*1, *2
Not Use



*1.*2
Not Use

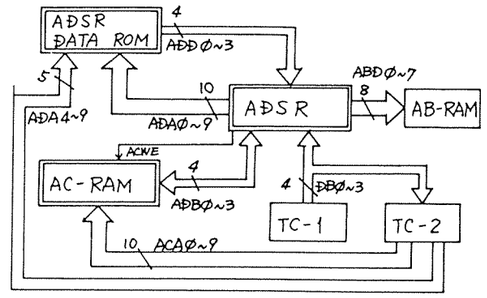
C2~4, 6~10, 13~15,
17, 19~42, 45~49,
:103





■ **AB-RAM · A-Series · B-Series · C-Series Block**

Formula-calculation Data (=ABDø ~ 7: Envelope Data) coming from ADSR is sent through 74LS367 to AB-RAM Block.
Timing for writing-in RAM is made in TC-2. It is determined by ABWE/A, B, C. ADSR Data are therefore distributed into A-Series, B-Series and C-Series by this Signal.
Data of A ~ H and a ~ h are sent out from AB-RAM to 74LS174 Latch circuit when ABWE/A, B, C is high level (which means read state).

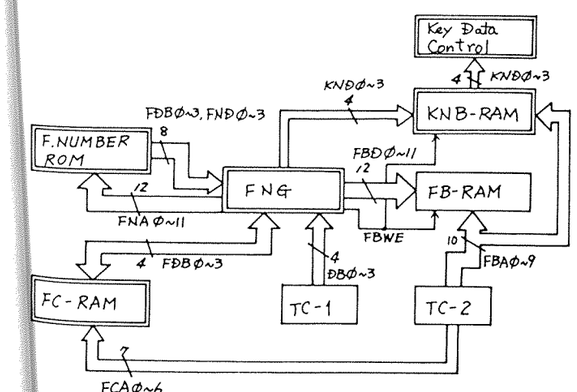


■ **ADSR · AC-RAM · ADSR DATA ROM Block**

ADSR Block makes out Address Signal (=ADAø ~ 9) to read out information irside ADSR DATA ROM by using DBø ~ 3 (. Key Note, Key ON-OFF etc.) sent from TC-1.
ADSR Data ROM Block outputs the Data (=ADDø ~ 3) to ADSR, which are ADSR SPEED, Phase information, ADSR Level data for changing the level of ADSR by depressed Key in range, etc.
These Data are read out by using above Address Signal (ADAø ~ 9) to read out the Address Signal ADA4 ~ 9; ADSR Speed, Attack, Release Phase end information etc.) coming from TC-2.
ADSR calculates the Data of ADDø ~ 3 and the Date of ADBø ~ 3 sent from AC-RAM and sends out the result to AB-RAM (=ABDø ~ 7). AC-RAM Block is used as temporary memory of final value of formula-calculation which is stored in the place of Address Signal (=ACAø ~ 9) made by TC-2 and is written by Write Signal (=ACWE) coming from ADSR.

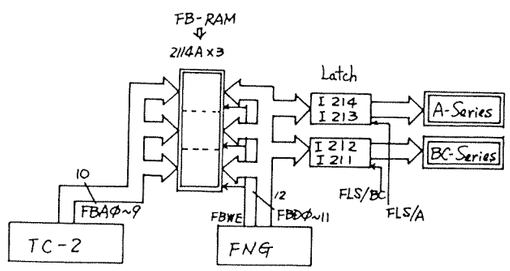
■ **TC-2 Block**

- Makes out the addresses of AC-RAM, AB-RAM, FC-RAM, FB-RAM and KNB-RAM by using the inside-counter.
- Output Data (ADA4 ~ 8) for Attack, Decay and Release Speed.
- Output Timing Signal (=ETCS) which is for transferring Effect Data (=DBø ~ 3) to AC-RAM.
- Output R/W Signal (=ABWE/A, B, C) of AB-RAM.



■ **FNG · FC-RAM · F. NUMBER ROM · KNB-RAM · Key Data Control Block**

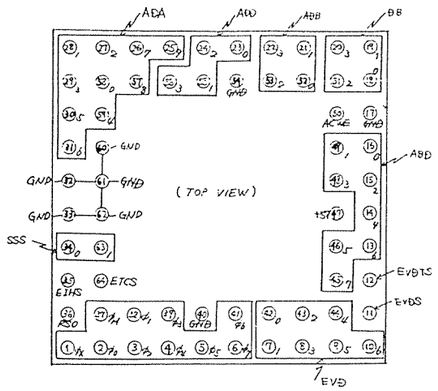
- FNG Block sends out Address Signal (=FNAø ~ 11) to read out the information (Frequency information responding to the depressed-key) inside F. Number ROM by using Key Note Information transferred from TC-1. F. Number ROM Block outputs the frequency information (=FDBø ~ 3, FNDø ~ 3) to FNG by FNAø ~ 11 described above.
- FNG calculates the frequency information and another information (=FDBø ~ 3) inputs from FC-RAM according to the formula and then outputs the result to FB-RAM. The Signal resulting from the formula-calculation is used as an address signal to read out the tone color wave-shape data.
- FC-RAM is used as a temporary memory to store the final calculated data of each channel of depressed-key in FNG. And FC-RAM outputs the Data to FNG when necessary.
- Concerning KNB-RAM Block, Key Note Data where tone is put into code from FNG is housed in the place of the Address Signal (=FBAø ~ 9) from TC-2.
  In Key Data Control Block, Key Note Code Octave Shift is carried out by using KNDø ~ 3 in order to select the filter that suits the tone tablet and depressed key.



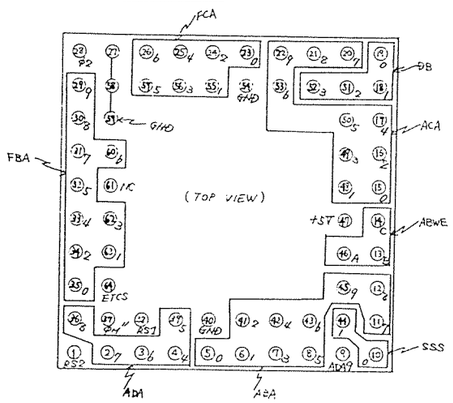
■ **FB-RAM · A-Series · BC-Series Block**

Formula calculation result (=FBDø ~ 11) from FNG is stored in the place of the Address (=FBAø ~ 9) coming from TC-2. Read/Write is carried out according to FBWE Signal. Output to A-Series and BC-Series when it is in Read. At this time, distribution into A-Series or BC-Series is performed according to Latch Signal FLS/A or/BC.

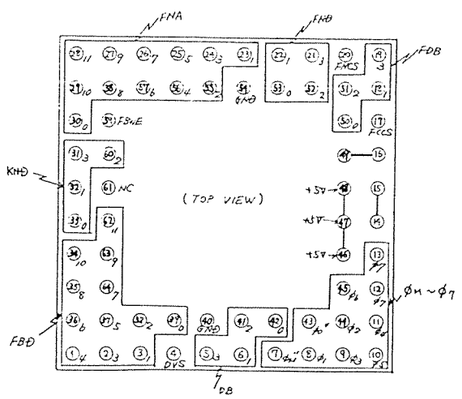
MB 60121C
LSI for ADSR Circuit



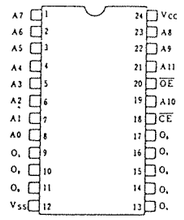
MB 62106C
LSI for TC-2 Circuit



MB 60120C
LSI for FNG Circuit

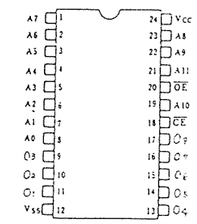


MB 8333 (MOS MASK ROM)
4096 x 8 Bit Read Only Memory
MB 8532, i 2332/2732 : PIN Compatible



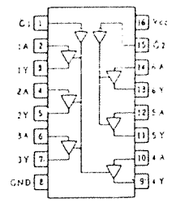
$A_0 \sim A_{11}$: Address Input
$O_1 \sim O_8$: Data Output
$\overline{CE}$: Chip Enable
$\overline{OE}$: Output Enable
Vcc : +5V
Vss : GND

MB 8333 (MOS MASK ROM)
4096 x 8 Bit Read Only Memory
MB 8532, i 2332/2732 : PIN Compatible



$A_0 \sim A_{11}$: Address Input
$O_1 \sim O_8$: Data Output
$\overline{CE}$: Chip Enable
$\overline{OE}$: Output Enable
Vcc : +5V
Vss : GND

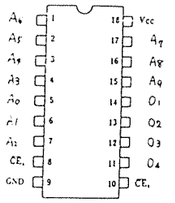
MB 74LS367
Hex Bus Driver



INPUT		OUTPUT
$\overline{G}$	A	Y
H	×	Z
L	L	L
L	H	H

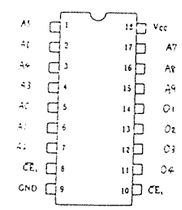
Z : High Impedance

MB 7054 (Bipolar Memory)
4096 - Bit Bipolar Programmable Read Only Memory (1024 x 4)
MB 7059 (Open Collector Output)
: PIN Compatible



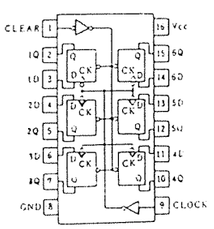
$A_0 \sim A_9$: Address Input
$O_1 \sim O_4$: Data Output
$\overline{CE}_1$, $\overline{CE}_2$: Chip Enable 1.2

MB 7054 (Bipolar Memory)
4096 - Bit Bipolar Programmable Read Only Memory (1024 x 4)
MB 7059 (Open Collector Output)
: PIN Compatible



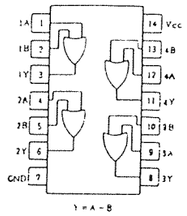
$A_0 \sim A_9$: Address Input
$O_1 \sim O_4$: Data Output
$\overline{CE}_1$, $\overline{CE}_2$: Chip Enable 1.2

MB 74LS174
Hex D-Type Flip-Flop with Common Direct Clear



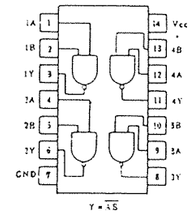
INPUT			OUTPUT
CLEAR	CLOCK	D	Q
L	×	×	L
H	↑	H	H
H	↑	L	L
H	L	×	Q_0

MB 74LS32
Quadruple 2-Input Positive-OR Gate



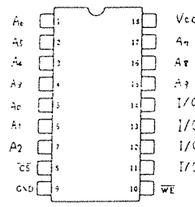
Y = A + B

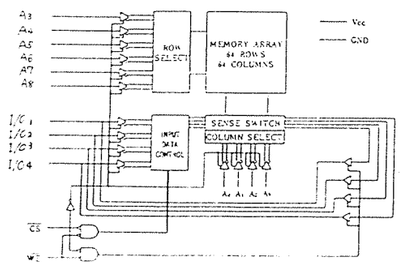
MB 74LS00
Quadruple 2-Input Positive-NAND Gate



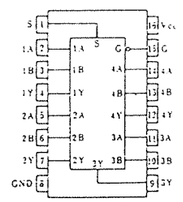
$Y = \overline{A \cdot B}$

μPD444C · MBM2114A-10L/15L
4096 Bit Static CMOS RAM





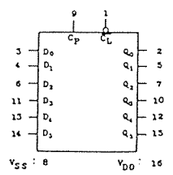
MB 74LS157
Quadruple 2-Line to 1-Line Data Selector/Multiplexer



INPUT				OUTPUT
G	S	A	B	Y
H	×	×	×	L
L	L	L	×	L
L	L	H	×	H
L	H	×	L	L
L	H	×	H	H

G : Strobe
S : Select

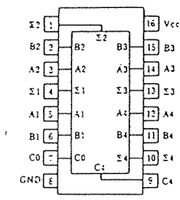
TC 40H174P
Hex D-Type Flip-Flop



INPUT			OUTPUT
CLOCK	D_n	CLEAR	Q_n
↑	H	H	H
↑	L	H	L
↓	*	H	No Change
*	*	L	L

* : Don't Care

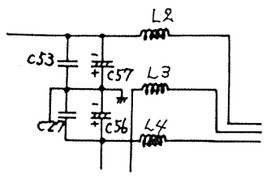
MB 74LS283
4-Bit Binary Full Adder

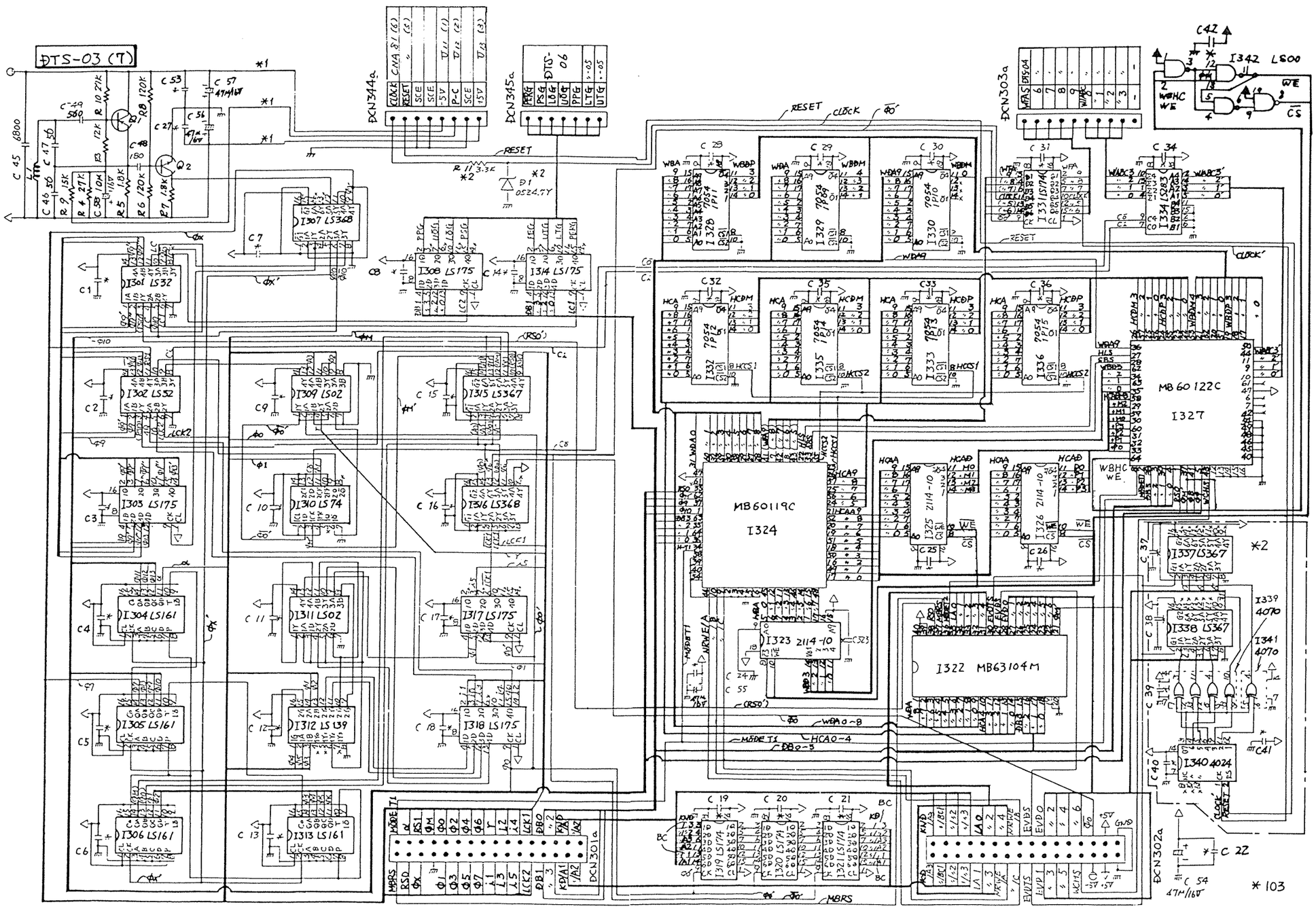


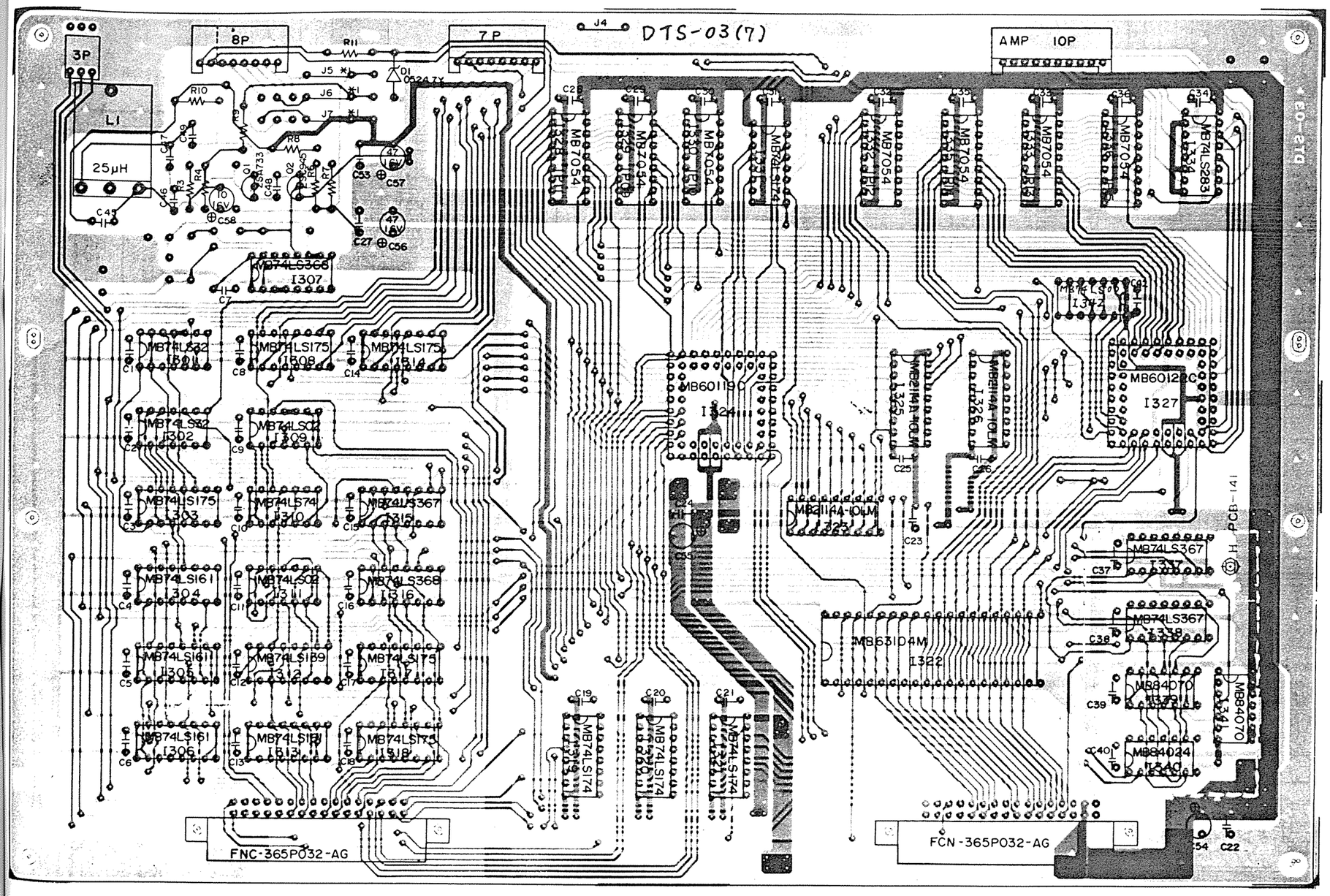
INPUT				OUTPUT					
				C_0 = "L" / C_2 = "L"			C_0 = "H" / C_2 = "H"		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	L	H	L	H	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	H	L	H	H	L
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

20. MASTER OSC · HCC · WFG CIRCUITS
DTS-03 (7)

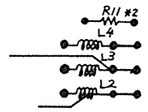
*1: In case of U.S.A., Canada Markets, show below

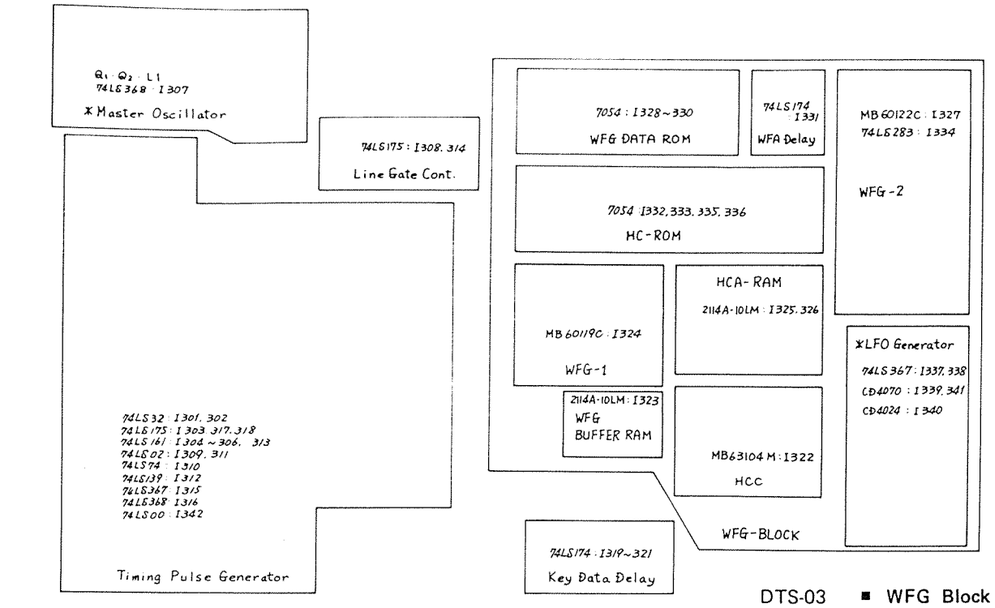




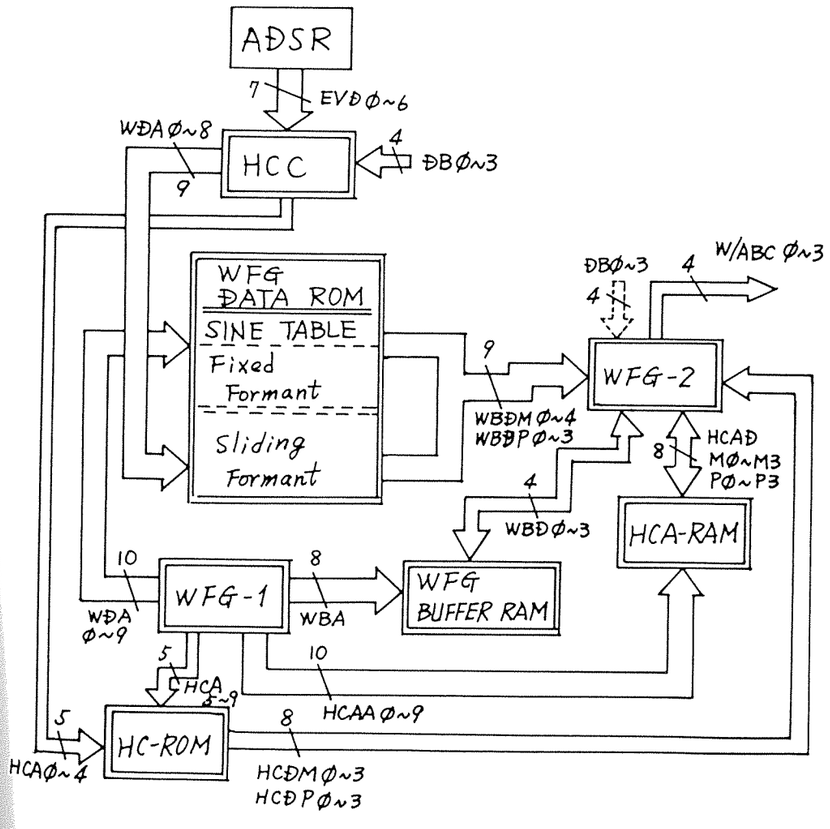


*1: In case of U.S.A. Canada Market, show bellow





DTS-03



■ WFG Block

WFG Block synthesizes wave form data by sine synthesis. The synthesis mode comes into the following 2 categories.

Mode I: Wave form (PP, P.S. St. Bass, Tuba)
Data Synthesis that changes in terms of time.

Mode II: Wave form (Tibia, Orchestra, Percus)
Data synthesis that does not change in terms of time.

Normally, formula-calculation of Mode I's wave form data sysnthesis is done, and that of Mode II's wave form data synthesis is performed when the next event occurs.

i) New Key is depressed "ON".
ii) When the Key is ON & Tablet or Controller etc. produces any changes.

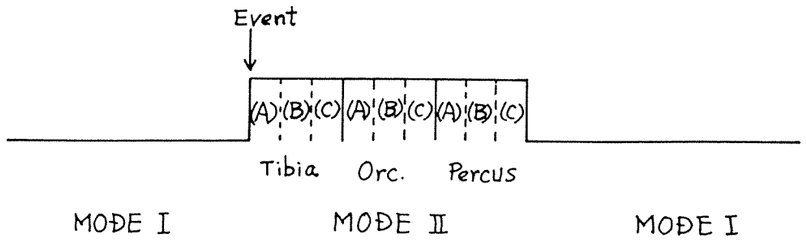
≪MODE I≫

HCC Block outputs address signal (=WDAϕ ~ 8) in order to read the desired data (= WBDPϕ ~ 3, WBDMϕ ~ 4: Sliding Formant data "SFD") out of WFG DATA ROM (: Sine Table, Fixed Formant, and Sliding Formant data are memorized) when Envelope Data (=EVDϕ ~ 6) from both DBϕ ~ 3 and ADSR Block is input.

WBDP and WBDM data are input to WFG-2 Block and temporarily stored in HCA-RAM Block as HCAD Mϕ ~ M3, Pϕ ~ P3.

HC-ROM Block outputs Harmonic coefficient data to WFG-2 after the upper address signal (=HCA5 ~ 9) coming from WFG-1 Block and lower address signal (= HCAϕ ~ 4) coming from HCC are input.

WFG-2 multiplies "SFD" by "C" that is stored in HCA-RAM and also multiplies the resulting numerical value by Sine Wave Form Data which is read out of the Sine Table inside WFG DATA ROM by address signal (=WDAϕ ~ 9) of WFG-1. The multiplied result (=WBDϕ ~ 3) is output to WF-RAM Block of DTS-04 through WFG BUFFER RAM and WFG-2 (=W/ABCϕ ~ 3).



≪MODE II≫

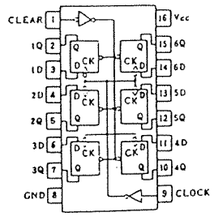
Formula-calculation of Mode II is carried out in the form of a cut-in as shown in the diagram above. And formula-calculation of Mode I is again performed after the formula-calculation of wave form data synthesis of Tibia system, Orchestra system and Percus are completed. The formula-calculation of Mode II goes through the following 3 steps ((A), (B), (C)).

(A): HCC Block outputs lower address signal (=HCAϕ ~ 4) to HC-ROM Block. When upper address signal (=HCA 5 ~ 9) is output to HC-ROM from WFG-1 Block, the desired high level wave coefficient (=HCDMϕ ~ 3, HCDP ϕ ~ 3), which is desired for each tone color among the desired Harmonic coefficient (=HCDMϕ ~ 3, HCDP ϕ ~ 3), whcih is desired for each tone among the data stored in HC-ROM is read out and output to WFG-2 Block.
the address signal (=WDAϕ ~ 8) of HCC from WFG DATA ROM. But in the formula-calculation of Mode II, Fixed Formant Data (=WBD Mϕ ~ 4, WBD Pϕ ~ 3) is read out and sent to WFG-2.
WFG-2 multiplies these data by the data (data to set the multiplied result within a given level) on DBϕ~ 3 and the result is temporarily stored in HCA-RAM Block.

(B): After the completion of (A)'s formula-calculation, Harmonic coefficients of same order with each tone are added by using (A)'s result (: Data stored in HCA-RAM), and it is temporarily stored in HCA-RAM.

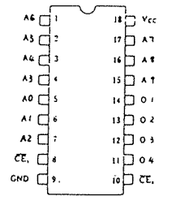
(C): After the completion of (B)'s formula-calculation, the address signal (= WDAϕ ~ 9) is output from WFG-1 to WFG DATA ROM. Then, the Sine Wave Form Data (=WBDMϕ ~ 4, WBDPϕ ~ 3) is output from the Sine Table of WFG DATA ROM to WFG-2 and multiplied by the data (=HCAP Mϕ ~ M3, Pϕ ~ P3) being temporarily stored in HCA-RAM when (B)'s formula-calculation is completed. The result of this formula-calculation is output to WF-RAM of DTS-04 through WFG BUFFER RAM and WFG-2.

MB74LS174
Hex D-Type Flip-Flop with Common Direct Clear



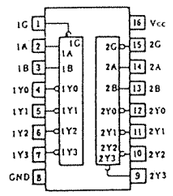
INPUT			OUTPUT
CLEAR	CLOCK	D	Q
L	×	×	L
H	↑	H	H
H	↑	L	L
H	L	×	Q_0

MB7054 (Bipolar Memory)
4096-Bit Bipolar Programmable Read Only Memory (1024 x 4)
MB7059 (Open Collector Output) : PIN Compatible



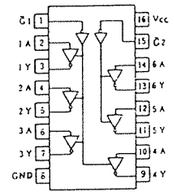
$A_0 \sim A_9$: Address Input
$O_1 \sim O_4$: Data Output
$\overline{CE}_1$, $\overline{CE}_2$: Chip Enable 1.2

MB74LS139
Dual 2-Line to 4-Line Decoder/Demultiplexer



INPUT			OUTPUT			
ENABLE G	SELECT B	SELECT A	Y0	Y1	Y2	Y3
H	×	×	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

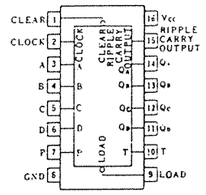
MB74LS368
Hex Bus Driver



INPUT		OUTPUT
$\overline{G}$	A	Y
H	×	Z
L	L	H
L	H	L

Z: High Impedance

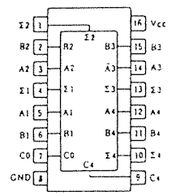
MB74LS161
Synchronous 4-Bit Binary Counter



MODE	INPUT						OUTPUT
	CLOCK	ENABLE P	ENABLE T	LOAD	CLEAR		
CLEAR	×	×	×	×	L		ALL "L"
PRESET	↑	×	×	L	H		PARALLEL IN
COUNT	↑	H	H	H	H		COUNT/CARRY
COUNT INHIBIT	×	H	L	H	H		HOLD
	×	L	H	H	H		

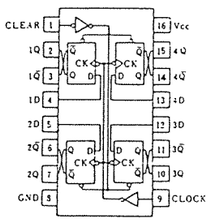
COUNT	OUTPUT				RIPPLE CARRY OUTPUT
	Q_A	Q_B	Q_C	Q_D	
0	L	L	L	L	L
1	H	L	L	L	L
2	L	H	L	L	L
3	H	H	L	L	L
4	L	L	H	L	L
5	H	L	H	L	L
6	L	H	H	L	L
7	H	H	H	L	L
8	L	L	L	H	L
9	H	L	L	H	L
10	L	H	L	H	L
11	H	H	L	H	L
12	L	L	H	H	L
13	H	L	H	H	L
14	L	H	H	H	L
15	H	H	H	H	H

MB74LS283
4-Bit Binary Full Adder



INPUT				OUTPUT					
A1	B1	A2	B2	Σ1	Σ2	C2	Σ1	Σ2	C2
A3	B3	A4	B4	Σ3	Σ4	C4	Σ3	Σ4	C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	L	H
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

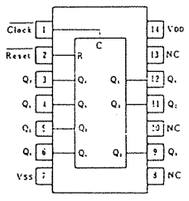
MB74LS175
Quadruple D-Type Flip-Flop with Common Direct Clear, Complementary Outputs



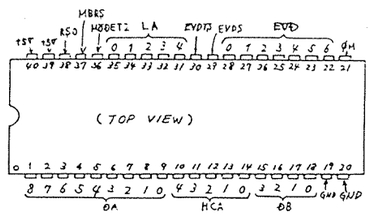
INPUT			OUTPUT	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	×	×	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	×	Q_0	$\overline{Q_0}$

↑ : "L" → "H"

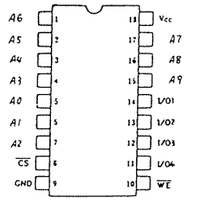
MB84024B
7-Bit Ripple-Carry Binary Counter
CD4024 AD.AK.AE.AF : PIN Compatible

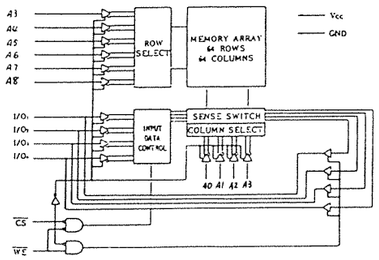


MB63104M
LSI for HCC Circuit

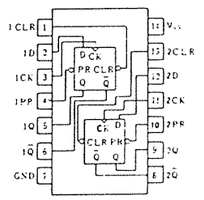


μPD444C · MBM2114A 10L/15L
4096 Bit Static CMOS RAM





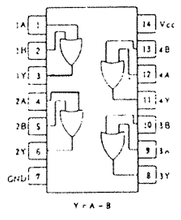
MB74LS74
Dual D-Type Positive-Edge-Triggered Flip-Flop with Preset and Clear



INPUT				OUTPUT	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	×	×	H	L
H	L	×	×	L	H
L	L	×	×	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	×	Q_0	$\overline{Q_0}$

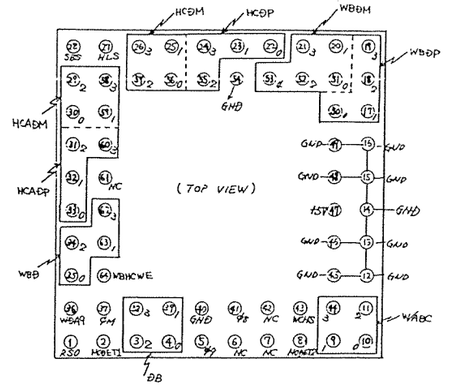
↑ : L → H
H*: UNCONSTANT → Q, $\overline{Q}$ "H"
PRESET & CLEAR "H" → Q, $\overline{Q}$ "H" or "L"

MB74LS32
Quadruple 2-Input Positive-OR Gate

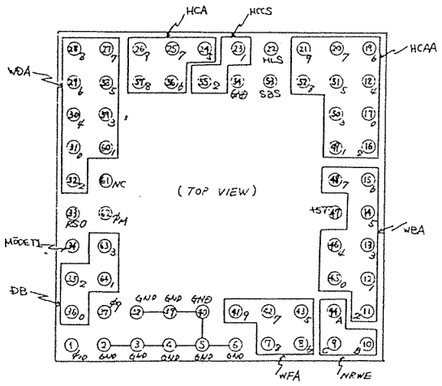


Y = A + B

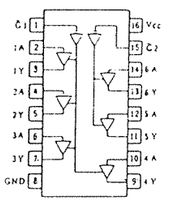
MB60122C
LSI for WFG Circuit



MB60119C
LSI for WFG Circuit



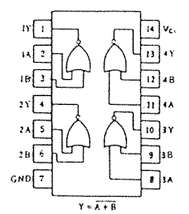
MB74LS367
Hex Bus Driver



INPUT		OUTPUT
$\overline{G}$	A	Y
H	×	Z
L	L	L
L	H	H

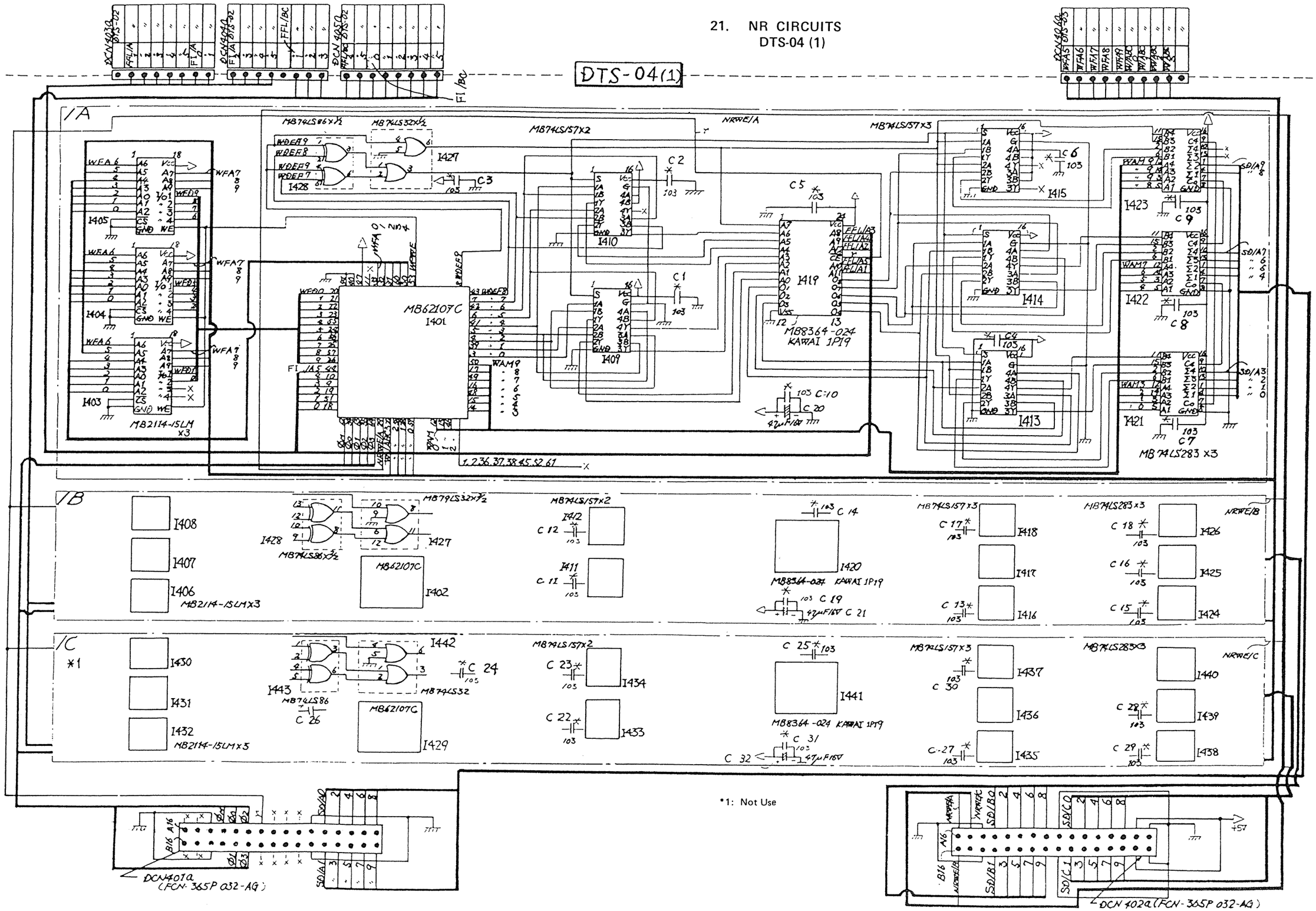
Z: High Impedance

MB74LS02
Quadruple 2-Input Positive-NOR Gate

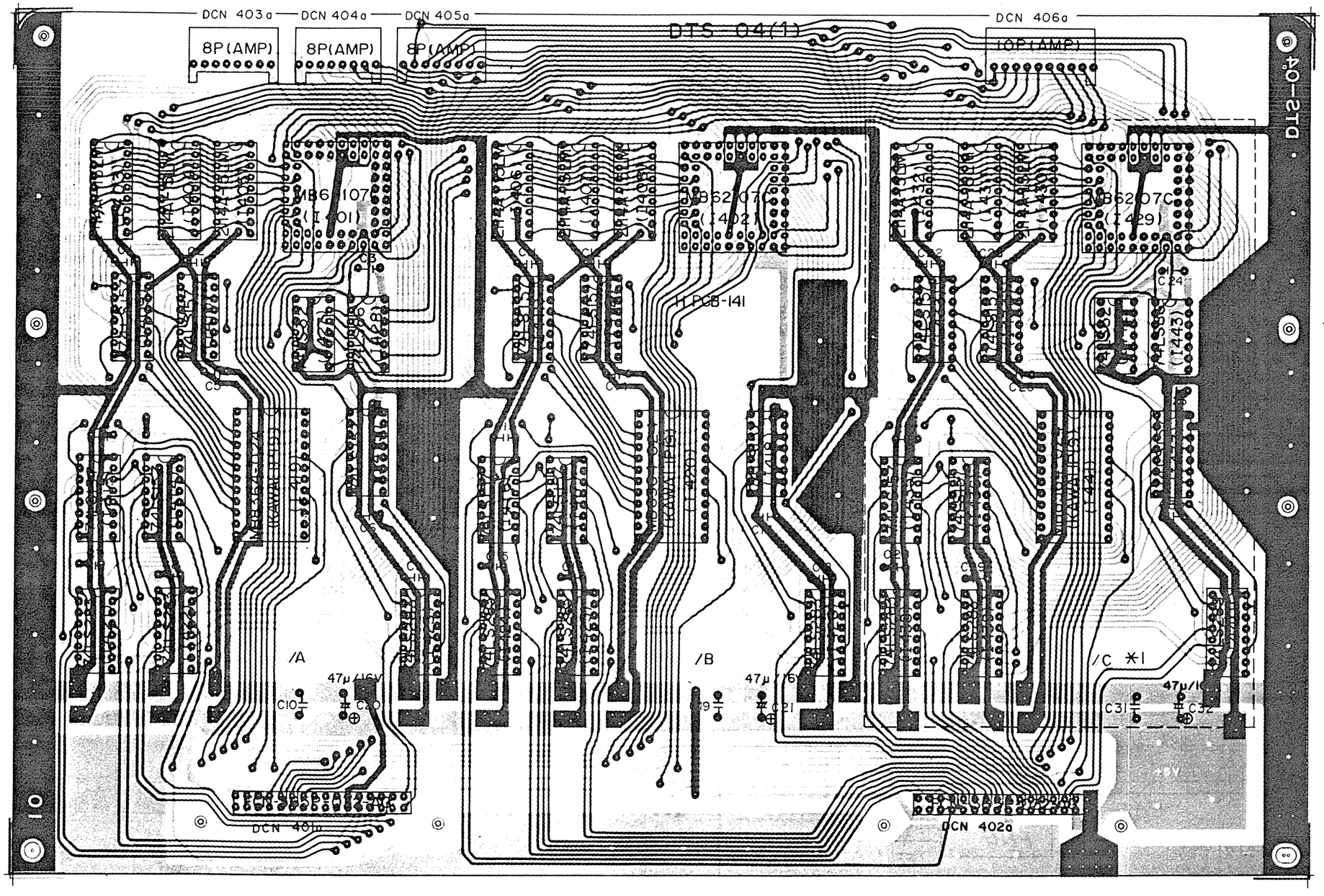


Y = $\overline{A+B}$

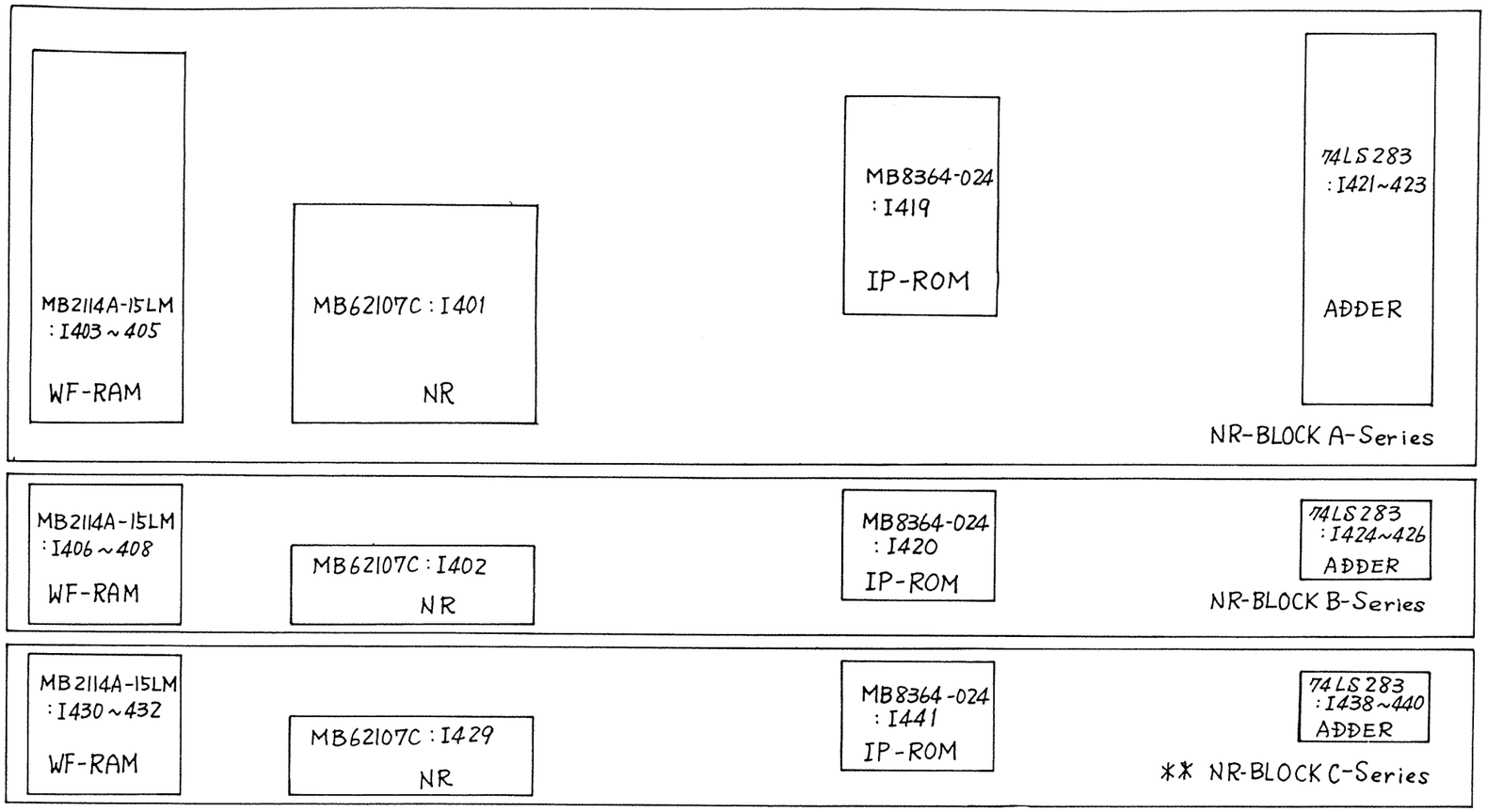
DTS-04(1)

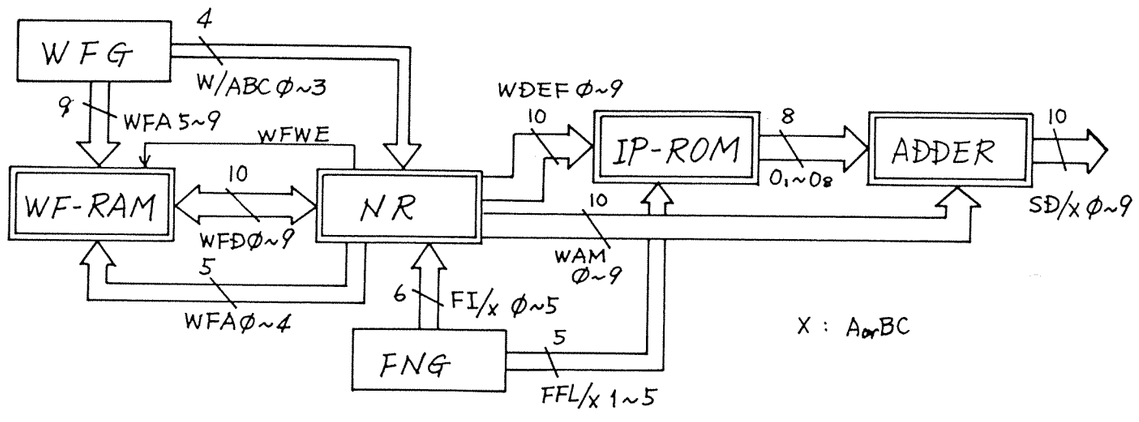


*1: Not Use


DCN 403a
DCN 404a
DCN 405a
DTS 04(1)
DCN 406a
8P(AMP)
8P(AMP)
8P(AMP)
10P(AMP)
MB6107
(I401)
MB62107C
(I402)
MB62107C
(I429)
74LS86
(I443)
11PCB-141
/A
47μ/16V
C10
C20
/B
47μ/16V
C19
C21
/C *1
47μ/16V
C31
C32
+5V
DCN 401a
DCN 402a
DTS-04
01

*1 : Not Use





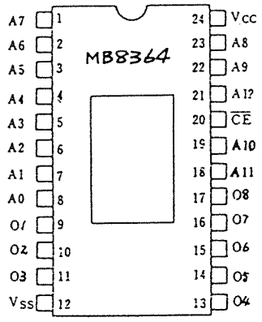
WF-RAM Block consists of 10 bits x 1024 Word and is capable of memorizing 32-point-wave form data with an amplitude of 10 bits. (This responds to the tone channel. Ex. Upper Orc. 8ch, Lower Orc. 7ch, Player Sound 8ch,... etc.)
Signal with 5 bits of WFA 5 ~ 9 addresses the Read or Write cycle to the kind. And 32-point-wave form is addressed by 5 bits of WFAφ ~ 4 coming from NR Block. (Output signal FI/xφ ~ 5 coming from FNG is dealt within NR in terms of formula-calculation and results in WFAφ ~ 4 that becomes a lower address for WF-RAM.)
WFWE signal is a control-signal to distinguish the condition of Read or Write of WF-RAM.

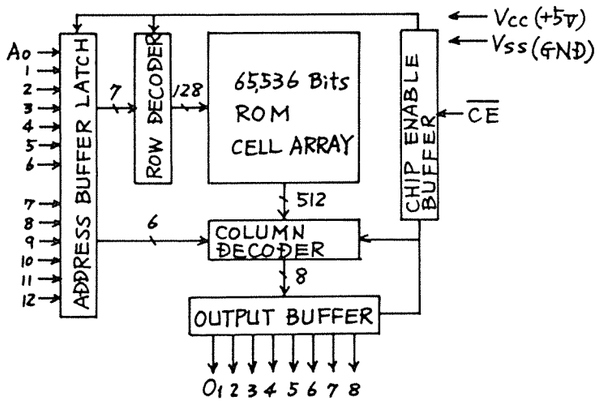
≪ Write Condition ≫
When wave form data (=W/ABCφ ~ 3) calculated in WFG is input to NR, the data is dealt in a serial (=10 bits). And if WFWE is "L", this data is temporarily stored in WF-RAM (=WFDφ ~ 9).
The Address signal at this time becomes the upper 5 bits (=WFA5 ~ 9) coming from WFG and the lower 5 bits (=WFAφ ~ 4) coming from NR.

≪ Read Condition ≫
Data (=WFDφ ~ 9), which is temporarily stored in WF-RAM, is read out and output to the ADDER Block as a data signal of WAMφ ~ 9 through NR when WFWE indicates "H". (FI/xφ ~ 5 signal is used to determine the address to read out the data of WFDφ ~ 9. Ref. DTS-02 FNG Block.)
The IP-ROM Block is used for interpolation. Address signal (=FI/xφ ~ 5), which is output from FNG, becomes WFAφ ~ 4.
Data, which is read out of WF-RAM, and another data by address +1 are dealt with in terms of formula-calculation in NR.
The result as a selecting signal (=WDEFφ ~ 9) of interpolation value is output to IP-ROM.
On the other hand, signal of FFL/x 1 ~ 5 from FNG is output to IP-ROM. This signal is used as data for the circuit to decrease digital noise of the wave form. And the signal indicates the phase value dividing between sample points of wave form data by 32 points.
between the wave form data and the sample is divided by 32.
Selecting signal (=WDEFφ ~ 9) of this phase value and interpolation value is used as the address of IP-ROM. The desired interpolation value is selected (= O_1 ~ O_8) and is output to the ADDER Block. This data is added to the said data of WAMφ ~ 9 and sent out to the next DAC & Filter circuit (DTS-05 or DTS-06) as data (=SD/x ~ 9) interpolated between samples.

▮ MB 8364

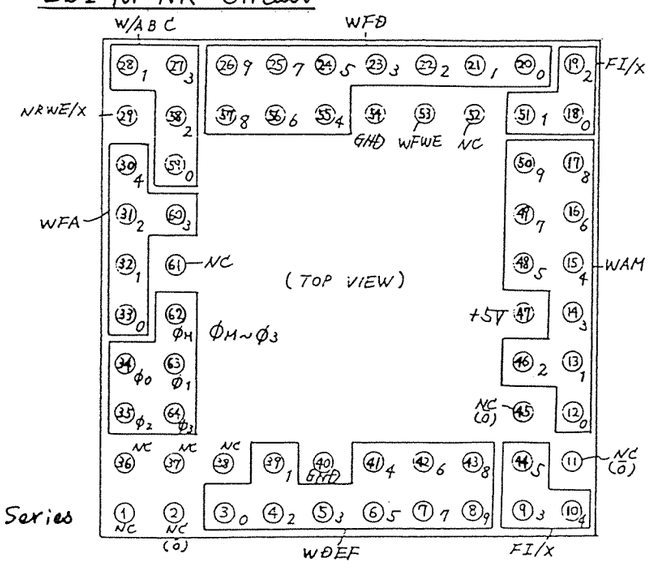
8192 x 8 Bit MASK ROM
EPROM TMS 2564 : Compatible





▮ MB 62107C

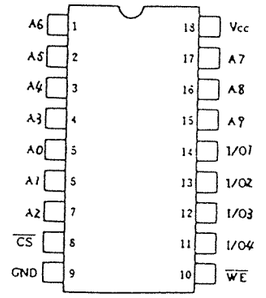
LSI for NR Circuit

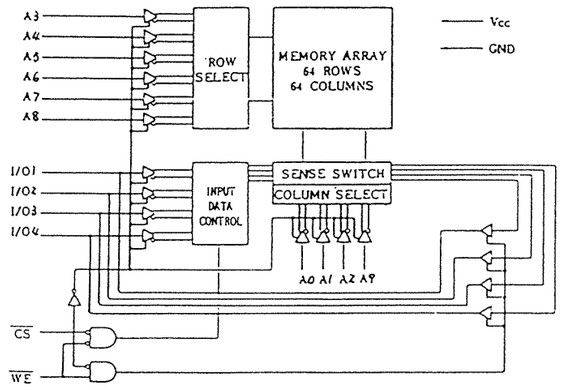


x : A or B or C Series

▮ μPD 444C · MBM 2114A–10L/15L

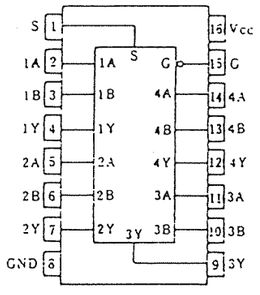
4096 Bit Static CMOS RAM





▮ MB 74LS157

Quadruple 2-Line to 1-Line Data Selector/ Multiplexer

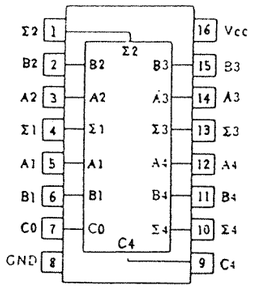


G : Strobe
S : Select

INPUT				OUTPUT
G	S	A	B	Y
H	×	×	×	L
L	L	L	×	L
L	L	H	×	H
L	H	×	L	L
L	H	×	H	H

▮ MB 74LS283

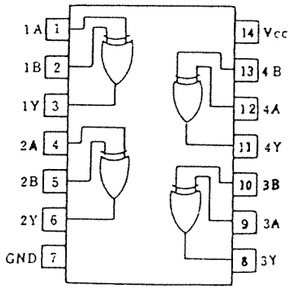
4-Bit Binary Full Adder



INPUT				OUTPUT					
				C0 = "L"			C0 = "H"		
				C2 = "L"			C2 = "H"		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

▮ MB 74LS86

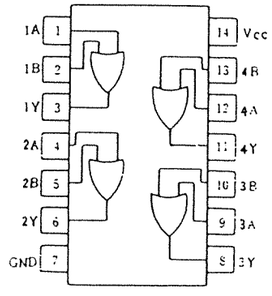
Quadruple 2-Input Exclusive-OR Gate



$Y = A \oplus B = \overline{A}B + A\overline{B}$

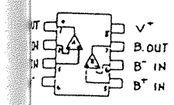
▮ MB 74LS32

Quadruple 2-Input Positive-OR Gate

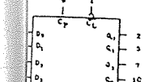


Y = A + B

NJM4558 DD
Dual OP-AMP



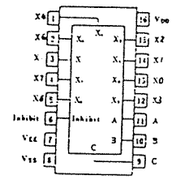
C 40H174P
Hex D-Type Flip-Flop



※ : Don't Care

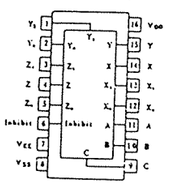
INPUT			OUTPUT
D	CLEAR	C	Q
H	H	↑	H
L	H	↑	L
※	H	↓	No Change
※	L	※	L

1 MB 84051 B
Single 8-Channel
Multiplexer/Demultiplexer
CD4051: PIN Compatible

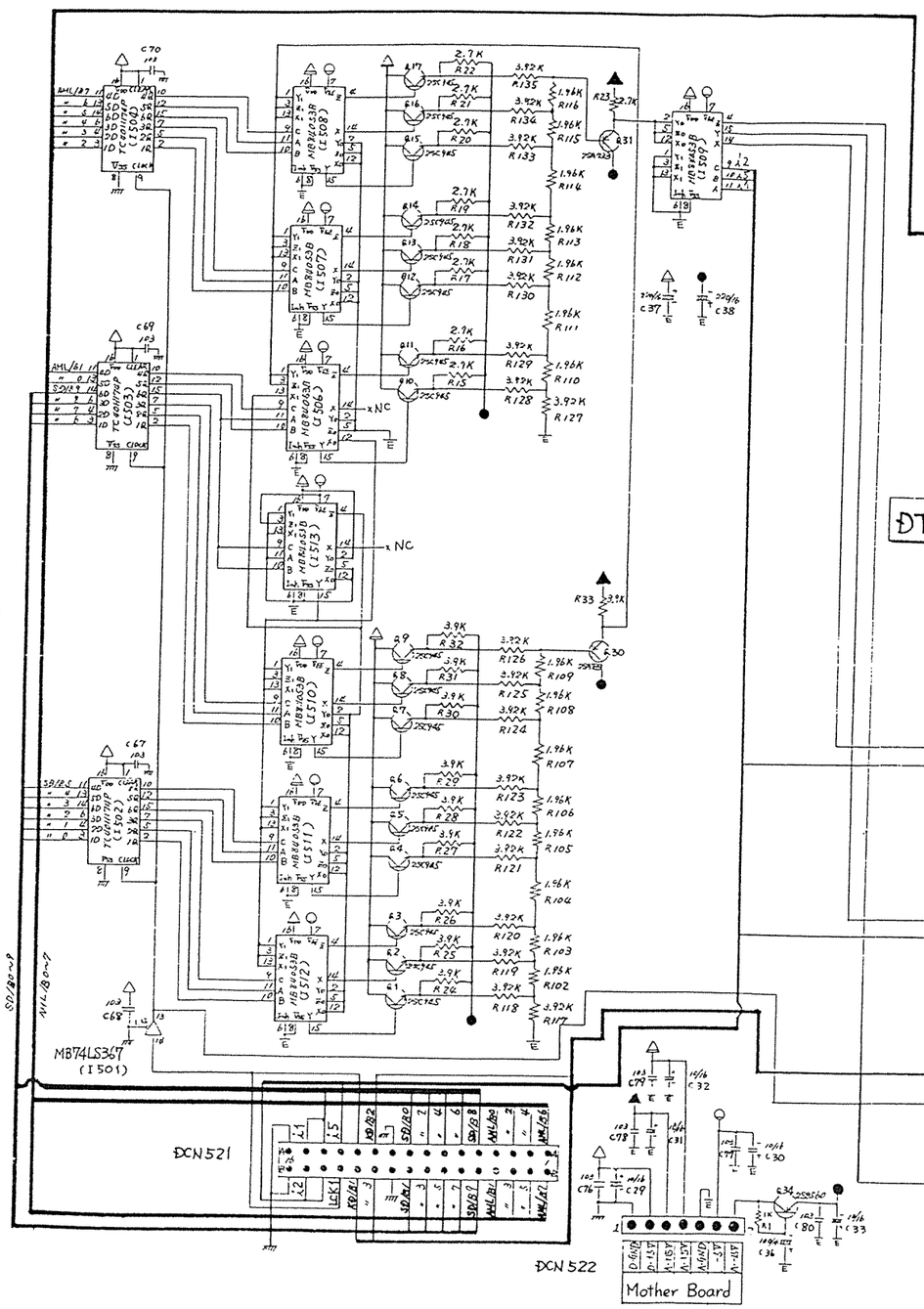


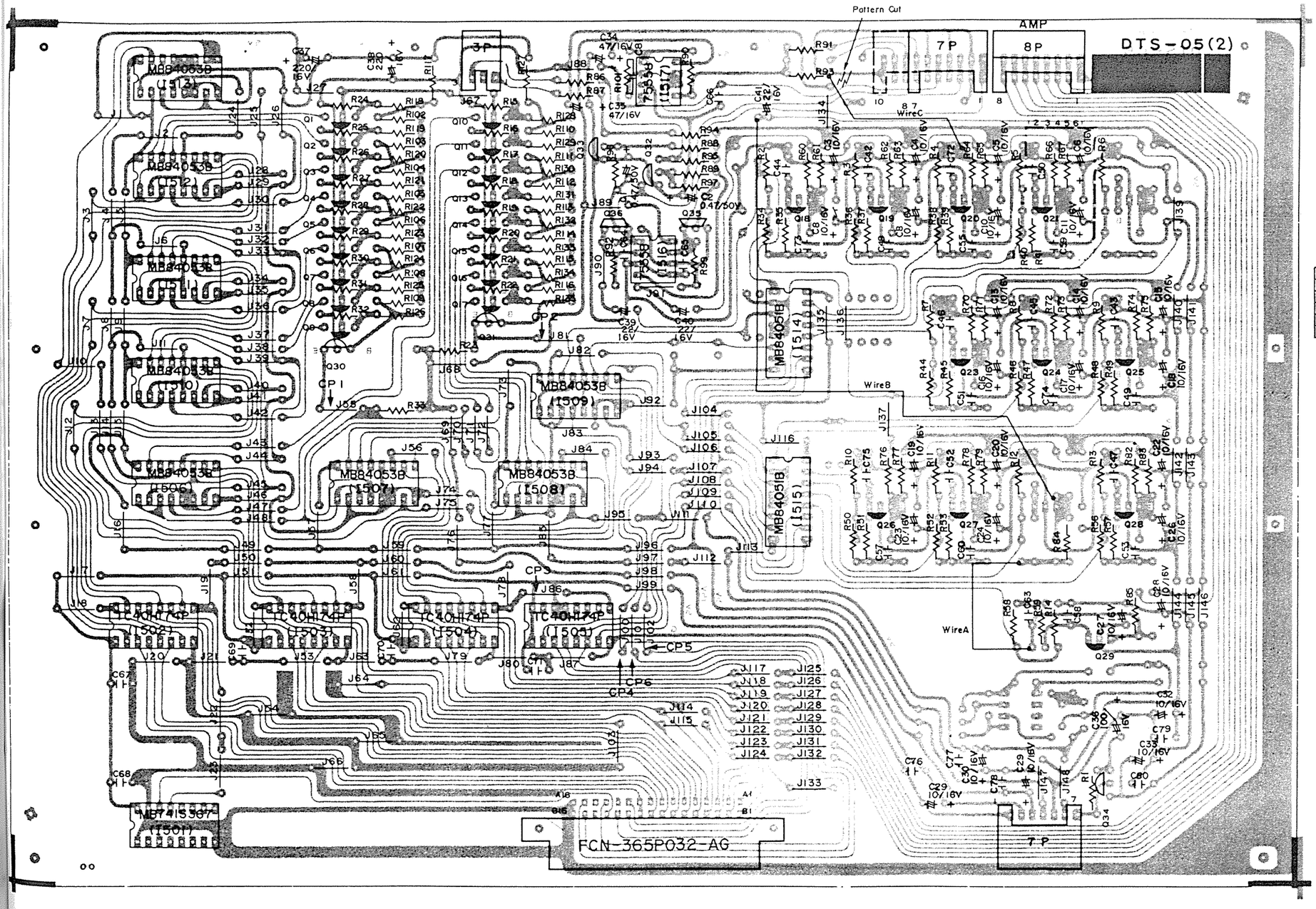
Control INPUT				ON Channel
INHIBIT	C	B	A	
0	0	0	0	X0
0	0	0	1	X1
0	0	1	0	X2
0	0	1	1	X3
0	1	0	0	X4
0	1	0	1	X5
0	1	1	0	X6
0	1	1	1	X7
1	※	※	※	—

1 MB 84053B
Triple 2-Channel
Multiplexer/Demultiplexer
CD4053: PIN Compatible

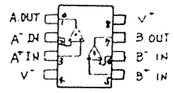


Control INPUT				ON Channel
INHIBIT	C	B	A	
0	0	0	0	Z0 Y0 X0
0	0	0	1	Z0 Y0 X1
0	0	1	0	Z0 Y1 X0
0	0	1	1	Z0 Y1 X1
0	1	0	0	Z1 Y0 X0
0	1	0	1	Z1 Y0 X1
0	1	1	0	Z1 Y1 X0
0	1	1	1	Z1 Y1 X1
1	※	※	※	—

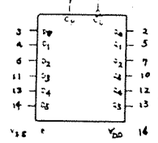




■ NJM4558DD
Dual OP-AMP



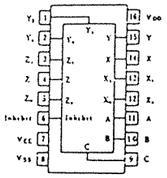
■ TC40H174P
Hex D-Type Flip-Flop



※ : Don't Care

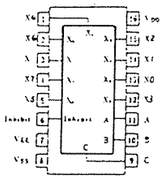
INPUT			OUTPUT
CLOCK	D_n	CLEAR	Q_n
↑	L	H	L
↑	H	H	H
L	●	H	NO Change
↓	●	L	L

■ MB84053B
Triple 2-Channel
Multiplexer/Demultiplexer
CD4053 : PIN Compatible



Control INPUT				ON
INHIBIT	C	B	A	Channel
0	0	0	0	Z, Y, X₀
0	0	0	1	Z, Y, X₁
0	0	1	0	Z, Y, X₂
0	0	1	1	Z, Y, X₃
0	1	0	0	Z, Y, X₄
0	1	0	1	Z, Y, X₅
0	1	1	0	Z, Y, X₆
0	1	1	1	Z, Y, X₇
1	×	×	×	—

■ MB84051B
Single 8-Channel
Multiplexer/Demultiplexer
CD4051 : PIN Compatible



Control INPUT				ON
INHIBIT	C	B	A	Channel
0	0	0	0	X₀
0	0	0	1	X₁
0	0	1	0	X₂
0	0	1	1	X₃
0	1	0	0	X₄
0	1	0	1	X₅
0	1	1	0	X₆
0	1	1	1	X₇
1	×	×	×	—

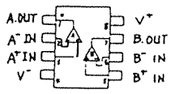
NOTE		DX500 Series	DX600 Series
*1	C81	100P	220P
*2	R101	680K	390K
*3	R99	220K	120K

*4 : DX600 Series ONLY

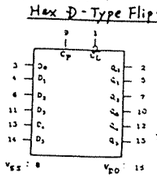
$Q_1 \sim Q_{21}$: 2SC945
$Q_{23} \sim Q_{29}$: 2SC945
$Q_{30} \sim Q_{33}$: 2SA733
Q_{34} : 2SB560
$Q_{35} \cdot Q_{36}$: 2SK44D

23. DAC & FILTER CIRCUITS FOR PLAYER SOUND
DTS-06 (1)

■ NJM4558DD
Dual OP-AMP

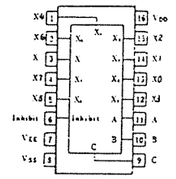


■ TC40H174P
Hex D-Type Flip-Flop



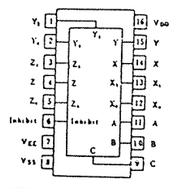
INPUT			OUTPUT
CLOCK	D_n	CLEAR	Q_n
↑	H	H	H
↑	L	H	L
↓	*	H	NO Change
*	*	L	L

■ MB84051B
Single 8-Channel
Multiplexer/Demultiplexer
CD4051: PIN Compatible



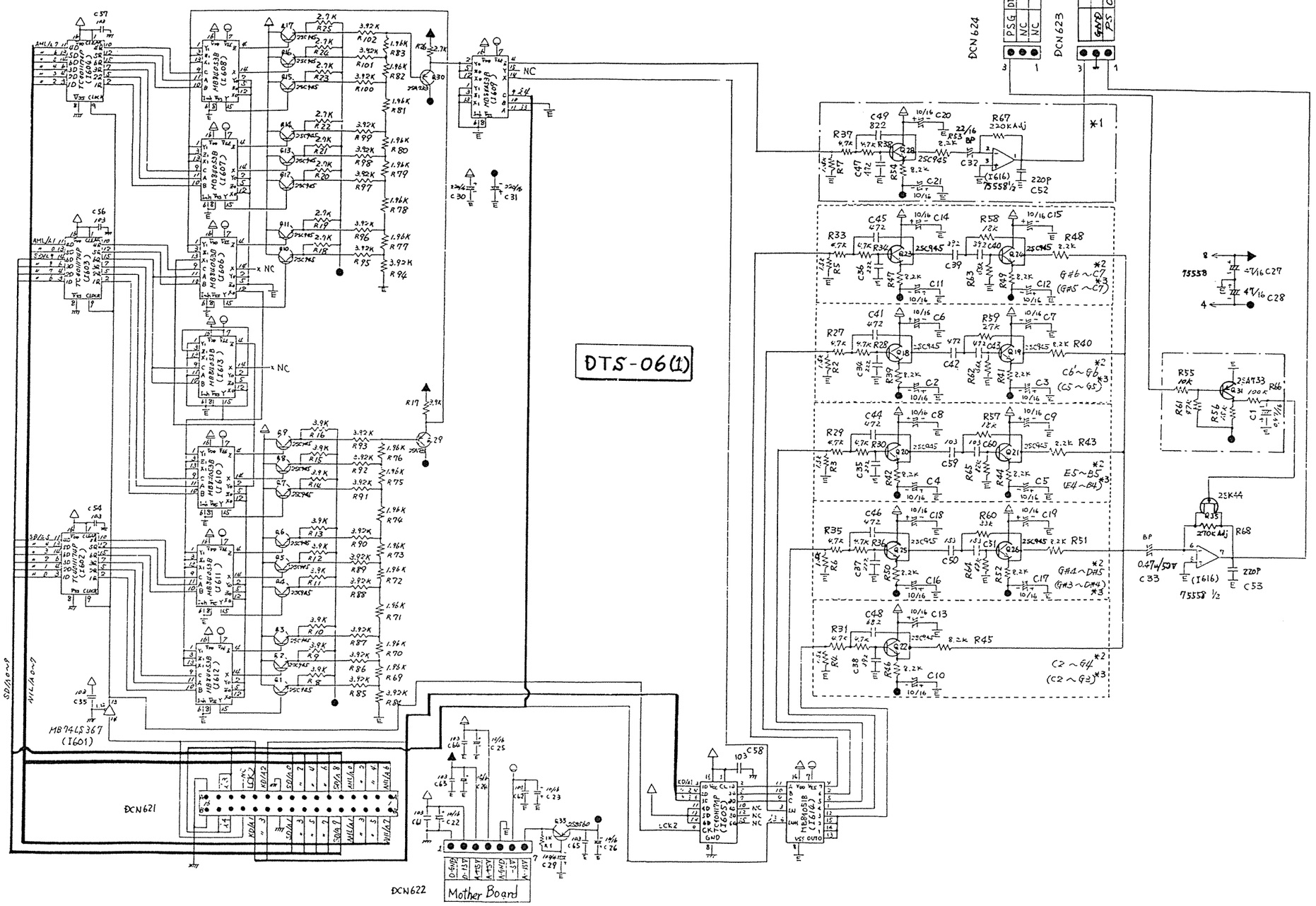
Control INPUT				ON Channel
INHIBIT	C	B	A	
0	0	0	0	X0
0	0	0	1	X1
0	0	1	0	X2
0	0	1	1	X3
0	1	0	0	X4
0	1	0	1	X5
0	1	1	0	X6
0	1	1	1	X7
1	*	*	*	—

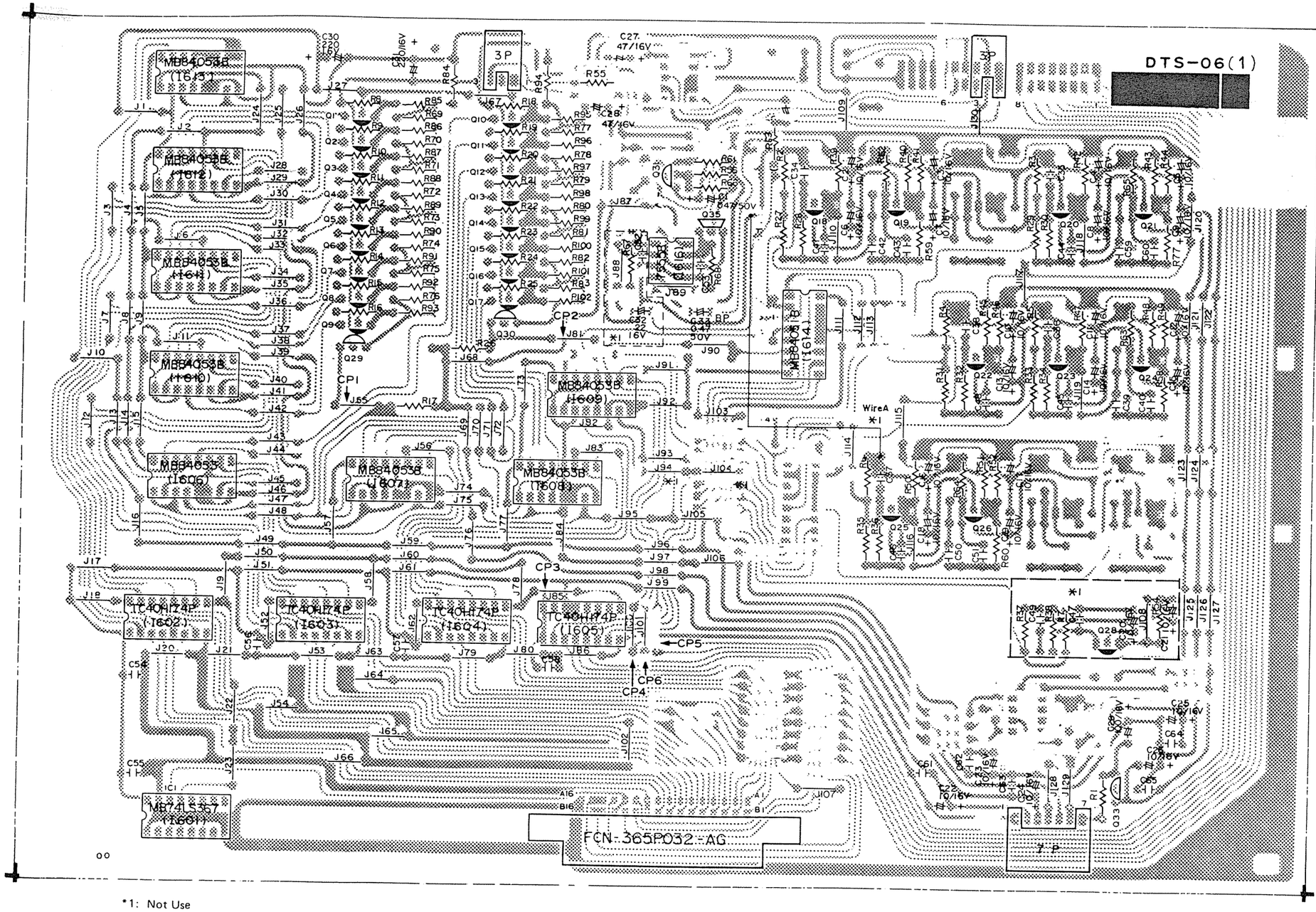
■ MB84053B
Triple 2-Channel
Multiplexer/Demultiplexer
CD4053: PIN Compatible



Control INPUT				ON Channel
INHIBIT	C	B	A	
0	0	0	0	Z_0 Y_0 X_0
0	0	0	1	Z_1 Y_1 X_1
0	0	1	0	Z_2 Y_2 X_2
0	0	1	1	Z_3 Y_3 X_3
0	1	0	0	Z_4 Y_4 X_4
0	1	0	1	Z_5 Y_5 X_5
0	1	1	0	Z_6 Y_6 X_6
0	1	1	1	Z_7 Y_7 X_7
1	*	*	*	—

*1: Not Use
*2: Keynote in case 16' voices are selected
*3: Keynote in case other voices than 16' ones are selected (connecting To Lower, To Pedal Button)





*1: Not Use

$Q_1 \sim Q_{26}, Q_{28}$	2SC945
$Q_{29} \sim Q_{31}$	2SA733
Q_{33}	2SB560
Q_{35}	2SK44D

LATCH (SD/B0 ~ 9 & AML/B0 ~ 7)

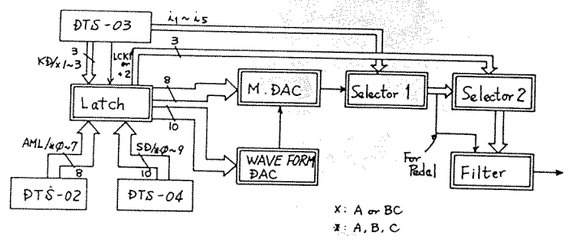
TC40H174P : I602 ~ 605

Note
I605 : KD/A1 ~ A3

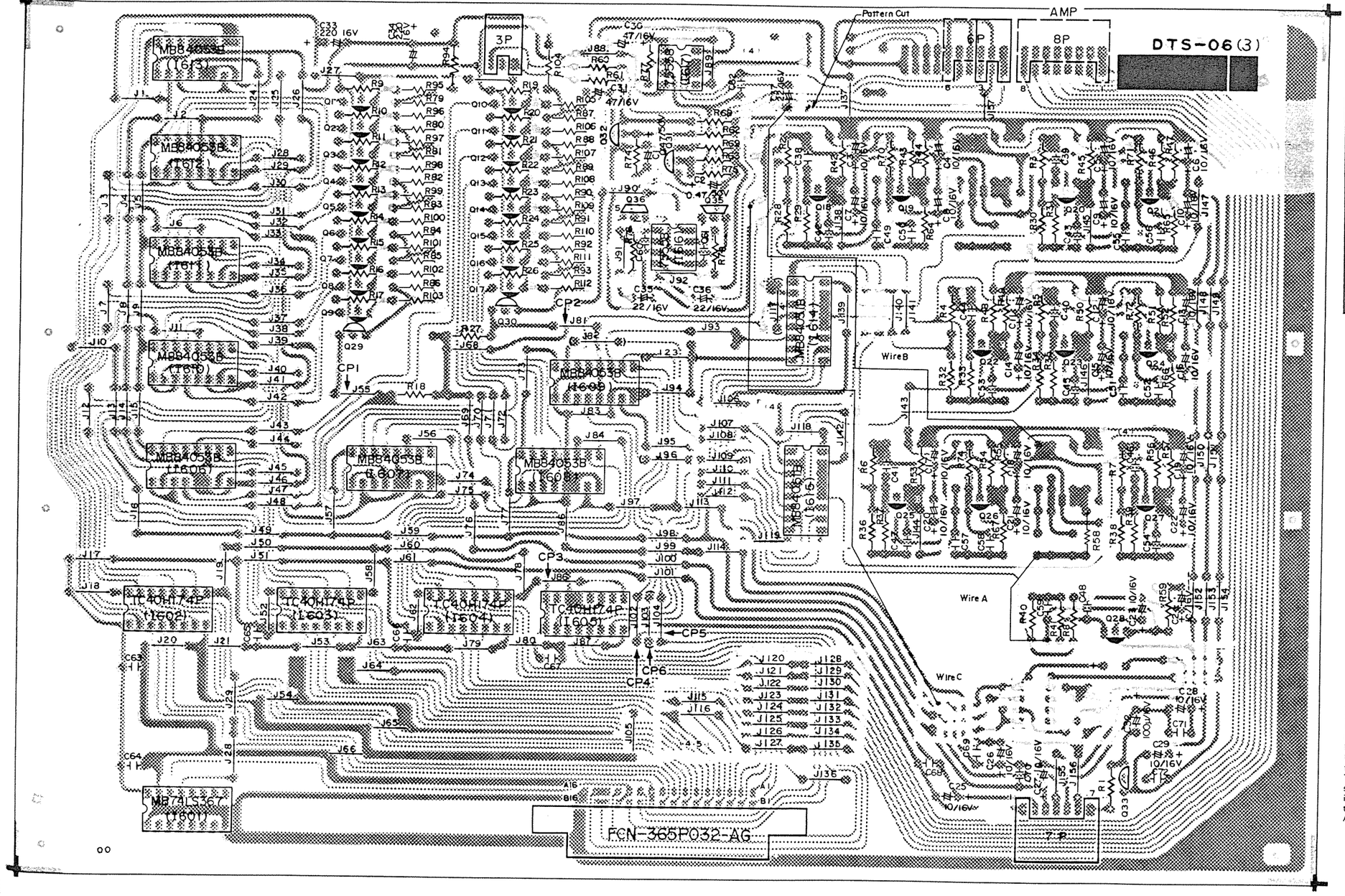
MB84053B : I606 ~ 608
$Q_{10} \sim Q_{17}, Q_{30}$
M. DAC
$R_{18} \sim R_{26}, R_{77} \sim R_{83}, R_{94} \sim R_{102}$

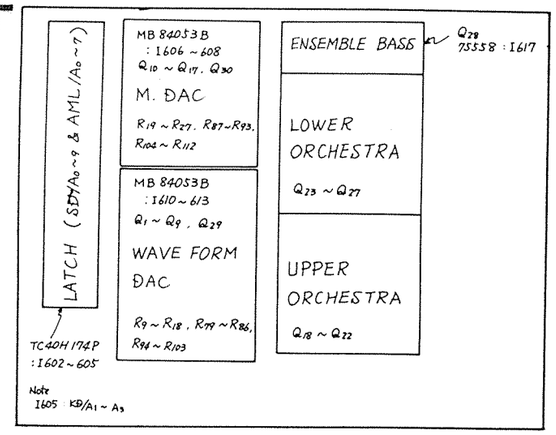
MB84053B : I610 ~ 613
$Q_1 \sim Q_9, Q_{29}$
WAVE FORM DAC
$R_8 \sim R_{17}, R_{69} \sim R_{76}, R_{84} \sim R_{93}$

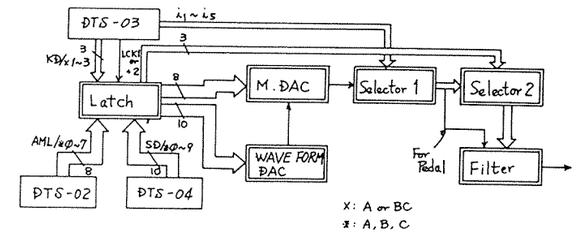
PLAYER SOUND
$Q_{18} \sim Q_{26}$



AML/Aφ ~ 7 (: ADSR Data) from DTS-02 and SD/Aφ ~ 9 (: Synthesized wave form Data) from DTS-04 are input to Latch Block.
These data signals carry out distribution into the next block by using the Latch Clock (=LCK2) from DTS-03 in order to select the desired tone among each series of tone.
Signal SD/Aφ ~ 9 is transmitted from Digital Data to Analog Data in WAVE FORM DAC Block and is output to M. DAC Block. (This Analog Data is used as reference voltage to determine the level of ADSR's amplitude.)
Digital signal AML/Aφ ~ 7 is transmitted to Analog Data in M. DAC Block as the function of WAVE FORM DAC. And the output-signal (musical tone wave form with ADSR) from this Block is sent to Selector 1 Block.
On the other hand, the Signal (= i_3, i_4 : Upper, Pedal), which selects a Keyboard's Filter Block among the Upper, Lower and Pedal, is input to this Block.
Musical tone wave forms coming from M. DAC are distributed by this signal each keyboard and sent to the next Block. The musical tone wave forms distributed into Upper and Lower are sent to Selector 2 Block, and if Pedal is selected, these wave forms are directly sent to the Filter Block without intervention of Selector 2 Block.
To Selector 2 Block, as well as these musical tone wave forms, Signal of 3 bits (A signal that latches Data Signal of KD/A 1 ~ 3 coming from DTS-03 in LCK2) is input from Latch Block. The signal of the 3 bits this time distributes the musical tone wave forms coming from M. DAC on the Upper keyboard or Lower keyboard. And the signal functions to make the filter circuit available.







AML/Aφ ~ 7 (: ADSR Data) from DTS-02 and SD/Aφ ~ 9 (: Synthesized wave form Data) from DTS-04 are input to Latch Block.
These data signals carry out distribution into the next block by using the Latch Clock (=LCK1) from DTS-03 in order to select the desired tone among each series of tone.
Signal SD/Aφ ~ 9 is transmitted from Digital Data to Analog Data in WAVE FORM DAC Block and is output to M. DAC Block. (This Analog Data is used as reference voltage to determine the level of ADSR's amplitude.)
Digital signal AML/Aφ ~ 7 is transmitted to Analog Data in M. DAC Block as the function of WAVE FORM DAC. And the output-signal (musical tone wave form with ADSR) from this Block is sent to Selector 1 Block.
On the other hand, the Signal (=i_1, i_2, i_3: U, L, P), which selects a Keyboard's Filter Block among the Upper, Lower and Pedal, is input to this Block.
Musical tone wave forms coming from M. DAC are distributed by this signal each keyboard and sent to the next Block. The musical tone wave forms distributed into Upper and Lower are sent to Selector 2 Block, and if Pedal is selected, these wave forms are directly sent to the Filter Block without intervention of Selector 2 Block.
To Selector 2 Block, as well as these musical tone wave forms, Signal of 3 bits (A signal that latches Data Signal of KD/A 1 ~ 3 coming from DTS-03 in LCK1) is input from Latch Block. The signal of the 3 bits this time distributes the musical tone wave forms coming from M. DAC on the Upper keyboard or Lower keyboard. And the signal functions to make the filter circuit available.

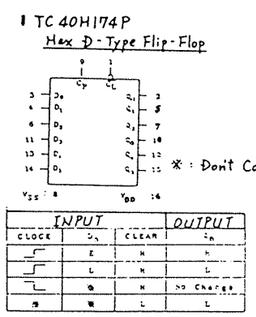
*1 Not Use

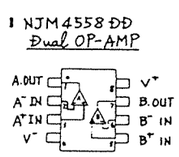
$Q_1 \sim Q_{28}$: 2SC945
$Q_{29} \sim Q_{32}$: 2SA733
Q_{33} : 2SB560
$Q_{35} \cdot Q_{36}$: 2SK44D

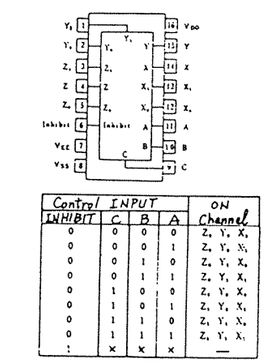
25. DAC & FILTER CIRCUITS FOR UPPER, LOWER ORCHESTRA & ENSEMBLE BASS DTS-06 (4)

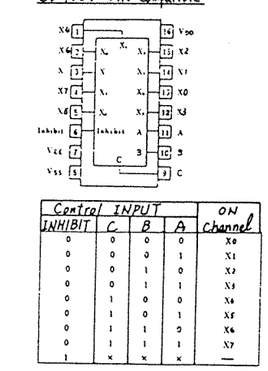
*1 : Keynote in case STRING 16' is selected in registration.

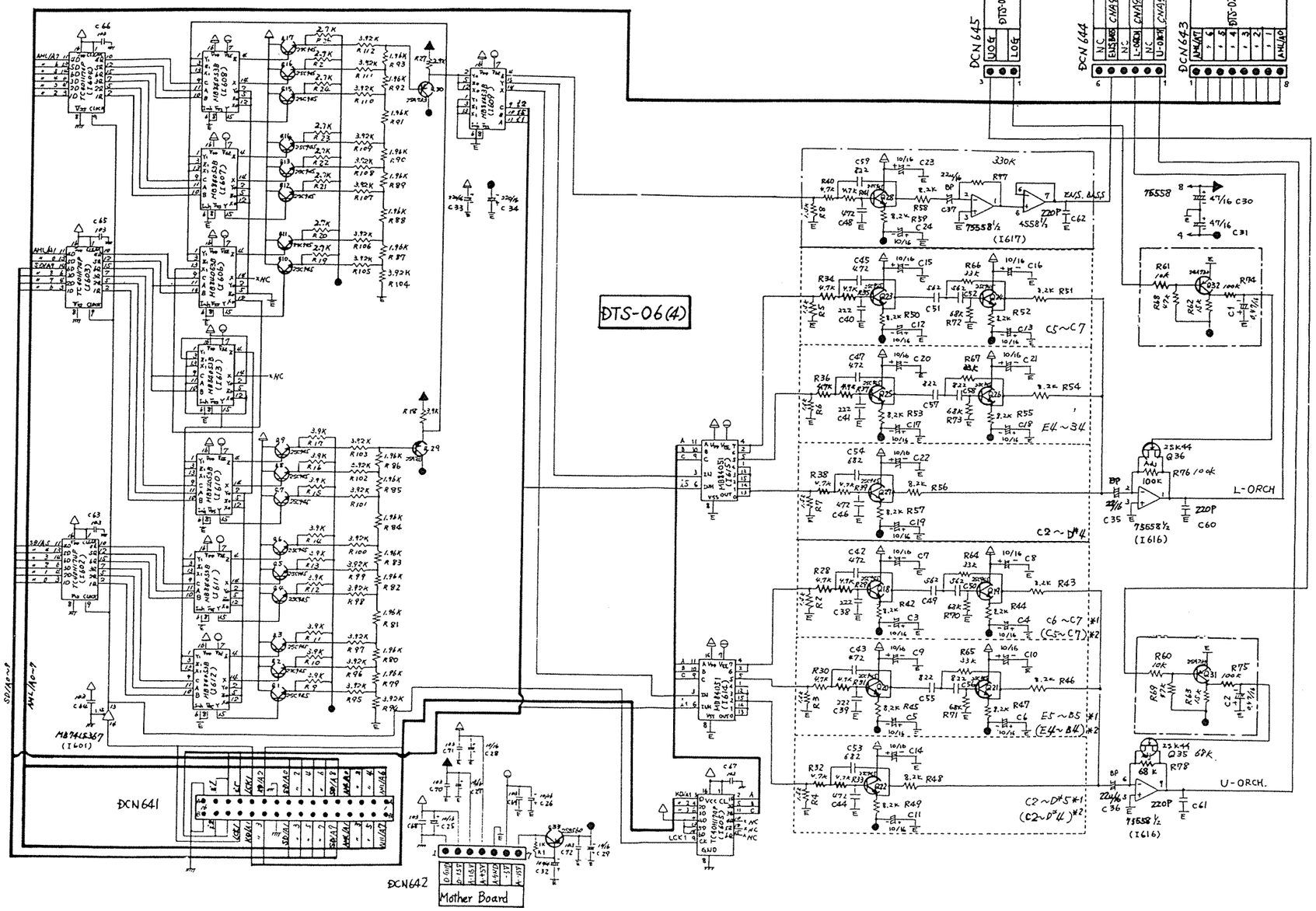
*2 : Keynote in case STRING 16' is not selected in registration.

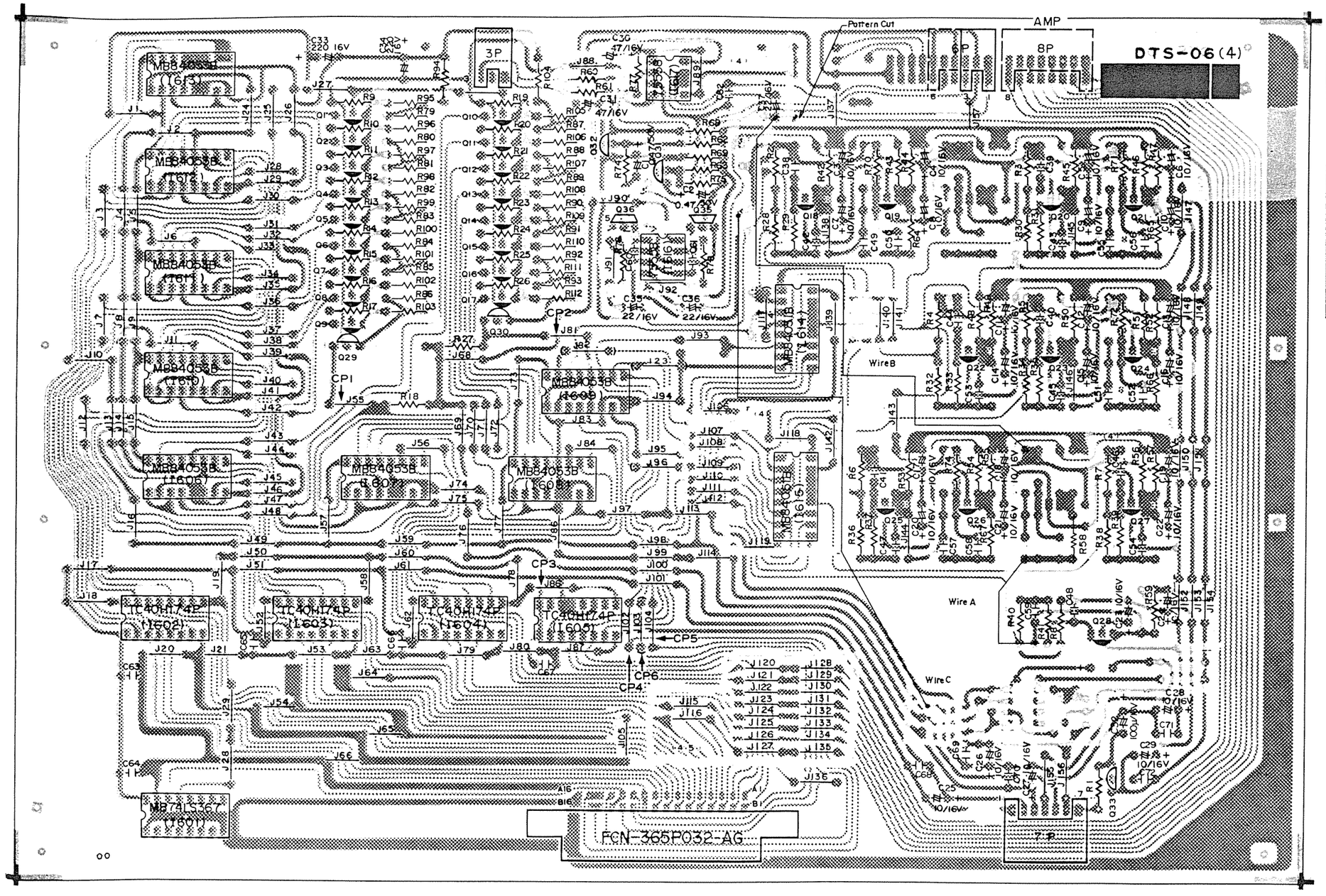


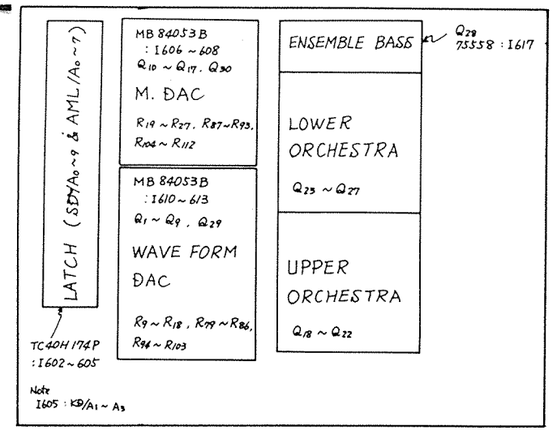


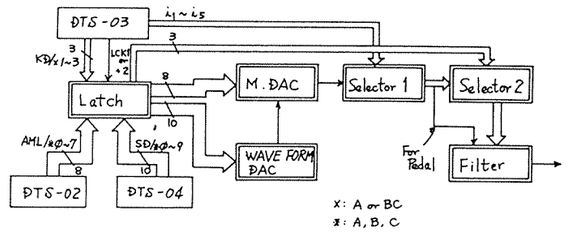












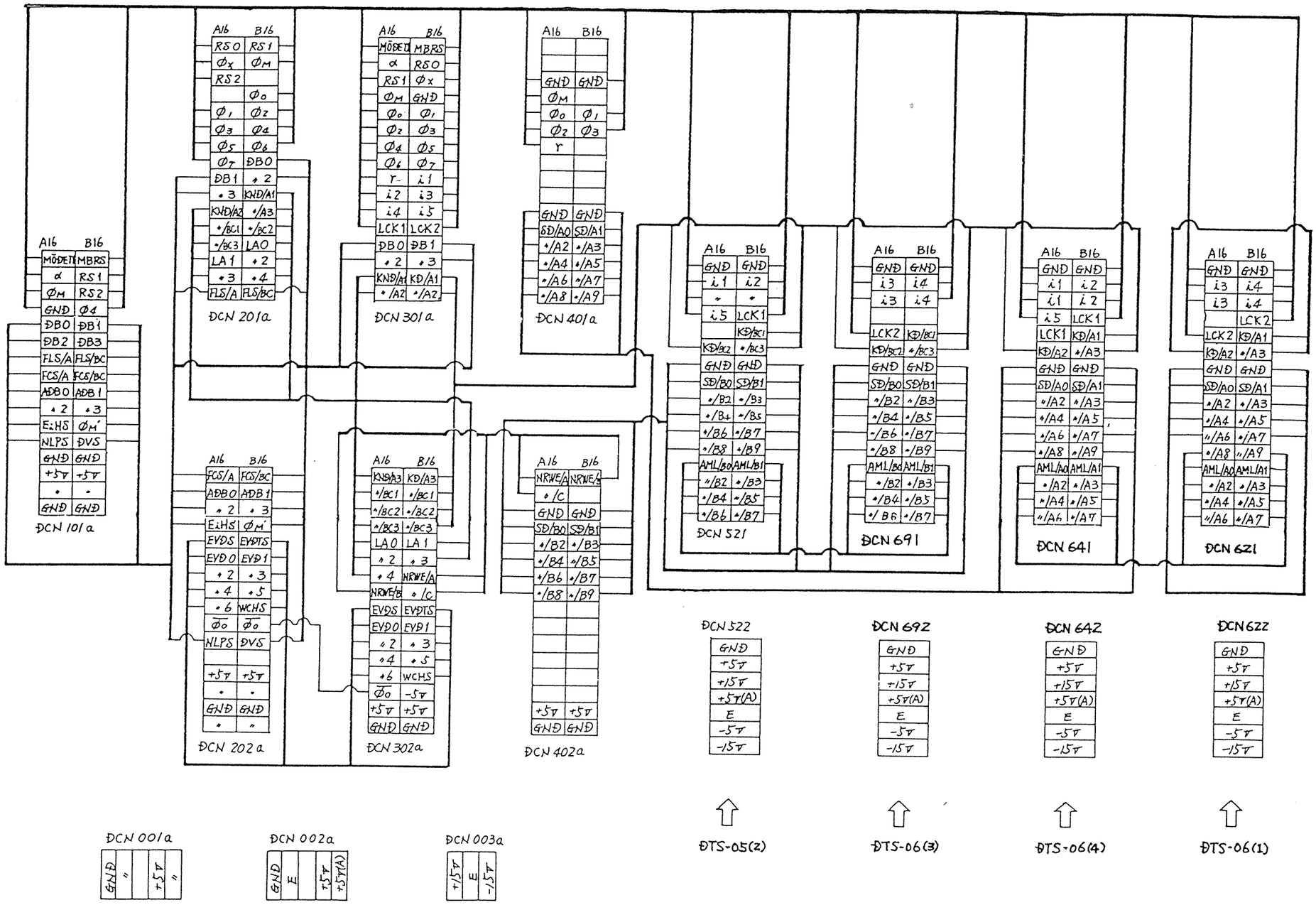
AML/Aφ ~ 7 (: ADSR Data) from DTS-02 and SD/Aφ ~ 9 (: Synthesized wave form Data) from DTS-04 are input to Latch Block.
These data signals carry out distribution into the next block by using the Latch Clock (=LCK1) from DTS-03 in order to select the desired tone among each series of tone.
Signal SD/Aφ ~ 9 is transmitted from Digital Data to Analog Data in WAVE FORM DAC Block and is output to M. DAC Block. (This Analog Data is used as reference voltage to determine the level of ADSR's amplitude.)
Digital signal AML/Aφ ~ 7 is transmitted to Analog Data in M. DAC Block as the function of WAVE FORM DAC. And the output-signal (musical tone wave form with ADSR) from this Block is sent to Selector 1 Block.
On the other hand, the Signal (=i_1, i_2, i_5: U, L, P), which selects a Keyboard's Filter Block among the Upper, Lower and Pedal, is input to this Block.
Musical tone wave forms coming from M. DAC are distributed by this signal each keyboard and sent to the next Block. The musical tone wave forms distributed into Upper and Lower are sent to Selector 2 Block, and if Pedal is selected, these wave forms are directly sent to the Filter Block without intervention of Selector 2 Block.
To Selector 2 Block, as well as these musical tone wave forms, Signal of 3 bits (A signal that latches Data Signal of KD/A 1 ~ 3 coming from DTS-03 in LCK1) is input from Latch Block. The signal of the 3 bits this time distributes the musical tone wave forms coming from M. DAC on the Upper keyboard or Lower keyboard. And the signal functions to make the filter circuit available.

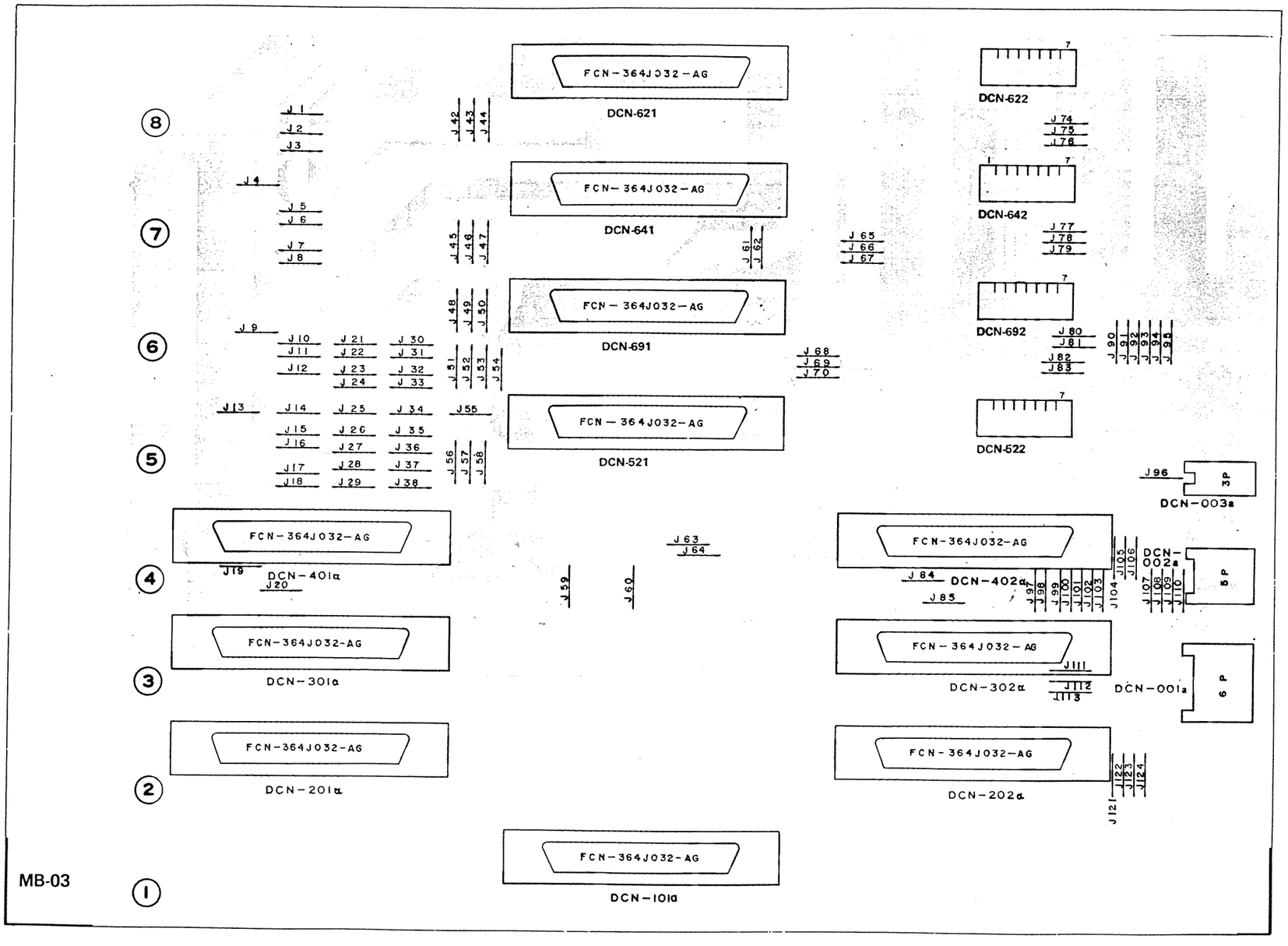
NOTE		DX500 Series	DX600 Series	DX700·DX1700· DX800·DX1800 Series
*1	R76	100K	68K	100K
*2	R77	330K	150K	330K
*3	R78	68K	47K	82K

*4 : DX500 Series ONLY

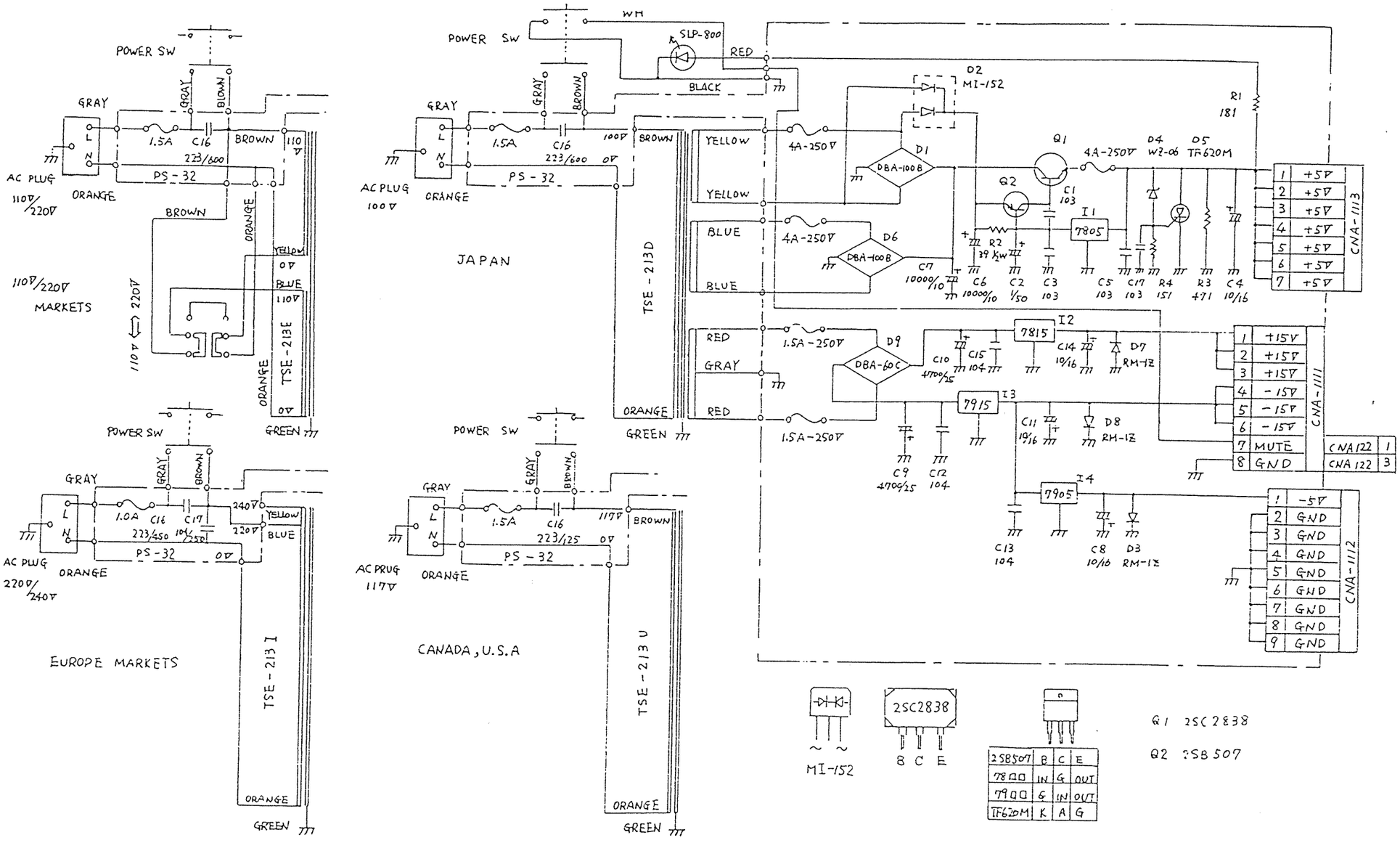
$Q_1 \sim Q_{28}$: 2SC945
$Q_{29} \sim Q_{32}$: 2SA733
Q_{33} : 2SB560
$Q_{35} \cdot Q_{36}$: 2SK44D

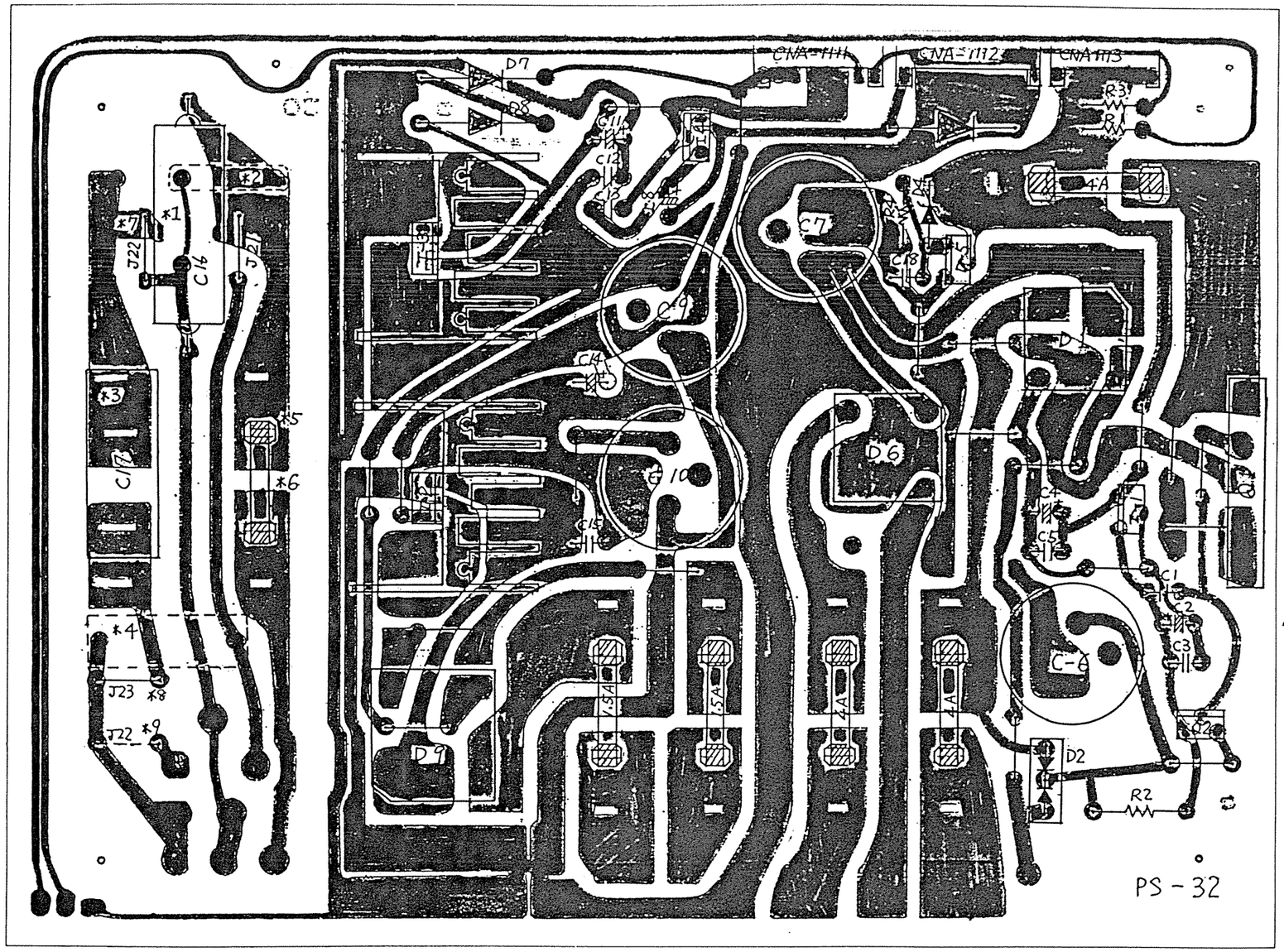
26. MOTHER BOARD
MB-03 (1)




8
7
6
5
4
3
2
1
FCN-364J032-AG
DCN-621
DCN-641
DCN-691
DCN-521
DCN-401α
DCN-301α
DCN-201α
DCN-101α
DCN-622
DCN-642
DCN-692
DCN-522
DCN-003α
DCN-402α
DCN-002α
DCN-302α
DCN-001α
DCN-202α
3P
5P
6P
MB-03

27. POWER SUPPLY CIRCUITS < PS-32 >





Item / Market	*1 (C16)	*2 (C16)	*3 (C17)	*4 (C16)	*5	*6	*7 (J22)	*8 (J23)	*9 (J22)
	Capacitor	Capacitor	Capacitor	Capacitor	Fuse Holder	Fuse	Jumper Line	Jumper Line	Jumper Line
Europe	223/400V (Oil)	Not Use	MP 10½/250V	Not Use	S-N5053	T-1A	Use	Use	Not Use
Japan	Not Use	223/600V	Not Use	Not Use	TF-01	1.5A	Not Use	Not Use	Not Use
Canada, U.S.A	Not Use	Not Use	Not Use	223/125V	TF-01	1.5A	Not Use	Not Use	Not Use
110V/220V	Not Use	223/600V	Not Use	Not Use	TF-01	1.5A	Not Use	Not Use	Use